Single electron memory devices based on nanocrystalline silicon dots

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Abstract
SiO$_2$/nc-Si/SiO$_2$ sandwich structure memory devices were prepared and thoroughly investigated by means of C-V and G-V measurements to clarify electron charging and discharging in nc-Si dots. Experiments showed that neither interface defects nor deep defects were dominant for the corresponding charging and discharging processes. Operation of a MOSFET single electron memory device using thus prepared sandwich structure as floating gate has been discussed in light of two different writing voltages. It is found that only one dot located over the channel determines its memory state where a threshold voltage shift of 92 mV corresponds to the trapping of one electron in the nc-Si dot. In our device the one electron retention state is found to be more stable than the two-electron one at 77 K.

I. Introduction
In the past decades, semiconductor quantum dot (QD) based science and technologies have been intensively investigated for their potential to novel device applications [1]. There has also been considerable as well as satisfactory progress in the understanding of both experimental and theoretical aspects of the transport properties of quantum dots [2]. A nanoscale quasi-nonvolatile metal oxide semiconductor field effect transistor (MOSFET) structure memory based on nanocrystalline silicon (nc-Si) dots is a fruit of such investigations, which possesses prospect for next generation digital data memory devices [3-6]. The nc-Si dots that are embedded in the oxide layer between a control gate and a channel act as floating memory nodes. Compared to the conventional stacked-gate flash memory, however, to overcome the leakage to drains through local defects, charges are not stored on a continuous floating-gate poly-silicon layer, but on a discontinuous floating-gate layer composed sparse nc-Si dots. In this kind of devices, few or even one electron guarantees a memory operation so that fast write/read/erase procedures as well as low power consumption are expected [7].

To prepare thus reliable memory, the floating memory node, nc-Si dot, and the channel structure are two of the most important factors. In our previous works, Ifuku et al. fabricated nc-Si dots with a narrow size distribution by very high frequency decomposition of silane (SiH$_4$) [8]. The used pulse reactant gas supply enables us to control the nucleation (density) and growth (diameter) of nc-Si dots. After located thus prepared nc-Si dots over a shot/narrow channel for an ideal single electron operation by remote deposition, a prototype MOSFET single electron device was proposed [9]. A shot/narrow channel here enables such device to be less affected by the randomness of nc-Si distribution and significantly reduces the scattering of electrical properties. Charge retention mechanism in floating nc-Si dots of the memory was discussed thoroughly [10, 11]. The lifetime of thus memory devices has been investigated by pulse-voltage measurements and explained through a model of an electron in a bound state of nc-Si dot with direct tunneling into the channel. Individual electron storage in the floating nc-Si dot has been observed. A possible stable memory state taking into multi-electron interaction account has been considered. Besides these fruitful efforts, we also realized that the retention mechanism of devices associated with interface defects or deep defects is still not clear though they strongly affect the overall actual device performance [12]. In this work, conductance-voltage (C-V) and conductance-voltage (G-V) methods have been utilized to sense and investigate electrons' write/store/erase properties as well as the effects of interface states. Kohno et al. studied the transient current of a Si quantum dot floating gate MOS structure and showed a charging and discharging process [13]. Effects of interface defects were not apparent in their work. On the other hand, Shi et al. claimed that deep level defects would often result in long-term retention...
behavior [14], whereas, Hinds et al. investigated the retention time distribution in MOSFET memory devices and concluded that interface defects did not play a dominant role in charge retention mechanism [10]. As a result of the discrepancy, further clarification on the retention mechanism and the role of interface defects is of utmost necessity. For an application, a MOSFET single electron memory device with narrow/short channel using thus sandwich structure as floating gate was discussed to give a more detail electron retention image corrected with device structure.

II. Experimental

For the sake of simplicity and representation, at first, a capacitor memory with a SiO$_2$/nc-Si/SiO$_2$ sandwich structure was prepared. The fabrication processes began with the <100> n-type silicon wafer (1-10 $\Omega\cdot$cm). An ultra-thin tunnel oxide (~2 nm thick) was grown by H$_2$SO$_4$/H$_2$O$_2$ oxidation. Next, a layer of uniform nc-Si dots with a diameter of 8±1 nm and a density of $1.2\times10^{11}$/cm$^2$ was deposited [8]. Subsequently a 60 nm thick upper oxide was grown by tetraethylorthosilicate (TEOS) PECVD method and the sample was annealed in N$_2$ ambient at 1100 $^\circ$C for 1 hour to improve the quality of TEOS SiO$_2$. Aluminum electrodes for the front (100 µm in diameter) and the back sides were evaporated after etching away the SiO$_2$ on the wafer backside, which also reduced upper oxide thickness to 54 nm. Finally, the sample was annealed again in H$_2$/N$_2$ ambient at 450 $^\circ$C, 5 min. For comparison, control samples without nc-Si dots were also fabricated following the same processes.

A MOSFET memory with short and narrow channel using thus prepared sandwich structure as a floating-gate was also prepared. Fabrication processes began with the dry-oxidation thinning of separation-by implanted-oxygen (SIMOX) silicon layer (p-type <100>) to 30 nm. Patterns for narrow and short Si channels (40 nm wide and 50nm long) are written by an EB lithography apparatus (JEOL JBX5 (FE)). The active area (narrow/short channel) of the device results from the proportionately higher resistance due to the smaller cross sectional area of the narrow channel. Using 50 µm wide leads reduces series resistance outside of gate area. Next, electron cyclotron resonance reactive ion etching (ECR-RIE) was used to transfer the resist pattern to the SOI layer. Subsequently ultra-thin tunnel oxide/nc-Si dots/gate oxide floating gate was prepared similar to that mentioned in sandwich structure memory. The fabricated sample contains 4 - 5 dots in the narrow/short channel. The other fabrications are same as CMOS standard procedures [15].

Scanning electron micrograph (SEM) and transmission electron micrograph (TEM) were utilized to observe microstructures of the samples. The electrical properties of the capacitor memory device and MOSFET single electron memories were measured by HP 4284A precision LCR meter and HP4156B precision semiconductor parameter analyzer respectively in the temperature range between 30 K to room temperature.

III. Results and Discussion

A schematic of the MOS capacitor with nc-Si as well as high-resolution TEM images are shown in Fig. 1. According to the low-resolution TEM image (Fig. 1b), a layer of uniform nc-Si dot is positioned at a constant distance (tunnel barrier) away from the silicon. A sparse distribution suppresses the lateral leakage current. High-resolution TEM (Fig. 1c) indicates that 8 nm nc-Si dots were sandwiched between 2 nm tunnel oxide and 54 nm upper gate oxide. A sheet density of $1.4\times10^{11}$ dots/cm$^2$ was measured by SEM observation.

The C-V and G-V characteristics are shown in Fig. 2. The C-V curves show a sharp transition from accumulation to inversion region.

![Fig. 1 a) The schematic of device structure. b) TEM image of sandwich structure. c) High-resolution image of nc-Si dot embedded in SiO$_2$.](image)
A clockwise hysteresis resulting from the switching of scan direction in depletion state was observed in both C-V and G-V characteristics. One also notices the presence of a conductance peak, whose position is close to the flat-band voltage, in either the forward or backward voltage sweep direction. Both the magnitude of the hysteresis in C-V and the shift in the peak positions in G-V are about 0.12 V. In contrast, no hysteresis in C-V characteristics or conductance peak in G-V characteristics was observed from the samples without nc-Si dots. Therefore these hysteresis and peak shift should be attributed to electron trapping into the sandwiched nc-Si or the interface on the nanocrystal dots, and not to defects in the oxide matrix or at the Si substrate/tunnel oxide interface. Further measurements also indicated that the clockwise hysteresis or the conductance peak shift is independent of the scan direction and speed (5 ~ 500 mV/s).

In our device, the Coulomb blockade effect can be very significant because of quantum size effect [1]. For our device, the Debye screening length at room temperature is about 74.8 nm, much larger than the average spacing between dots. Thus, even with a random distribution of dots in position, the lateral inhomogeneity in the band bending is unimportant for the operation of a memory device, even with charge loss from some of the dots. Based on our experimental results, at sufficiently large negative voltage (erasure voltage), no electron resides in the nc-Si dots and the neutral charge state is achieved. When the gate voltage is swept to a high positive value, a number of electrons will be stored in the nc-Si dots by direct tunneling through the ultra-thin oxide, resulting in the shift in the capacitance as well as the conductance characteristics. In the G-V measurements, nc-Si dot trap levels are detected through the ac loss resulting from a change in their occupancy produced by a small modulation of the gate voltage. This each ac loss could manifest itself as a conductance peak in G-V characteristics [16].

According to a model of fixed oxide charges [3], one can estimate the theoretical magnitude of flat-band shift ($\Delta V_{FB}$) with the formula

$$\Delta V_{FB} = \frac{en_{dot}}{\varepsilon_{ox}} (t_{upper} + \frac{1}{2} \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{dot})$$

where $n_{dot}$ is the density of the nc-Si, $t_{upper}$ is the upper gate oxide, $t_{dot}$ is the nc-Si dot diameter, $\varepsilon_{ox}$ and $\varepsilon_{Si}$ are the permittivities of oxide and silicon, respectively. From this formula, $\Delta V_{FB}$ is calculated for the present density of dots to be 0.282 V for one electron per nanocrystal. The experimentally measured flat-band shift, $\Delta V_{FB}$ = 0.12 V, under large positive gate voltage, thus suggests that less than one half of the nc-Si dots are charged.

For a better understanding of the results obtained from C-V and G-V measurements, the frequency dependence of the capacitance and conductance characteristics was investigated at various temperatures. The similar flat band voltage shift ($\Delta V_{FB}$) and conductance peak full width at half maximum (FWHM) in magnitude were found, which suggests that the hysteresis and the conductance peak have the same origin [17]. In the present experiments, both C-V and G-V characteristics are neither dispersed nor distorted with different frequencies and temperatures, which indicate that the interface state density is low, as it generally give rise to time- or frequency-dependent C-V and G-V characteristics [16]. It should be emphasized that the occurrence of the conductance peak observed in our experiments should be associated with the ac loss due to capture and emission of electrons by the nc-Si dots but not to the Si substrate/tunnel oxide interface states [18]. In references 18, a conductance peak with large FWHM was attributed to a large interface state density, with the continuum energy distribution of the interface states corresponding to the dispersion or distortion observed in C-V characteristics.

In order to investigate the influence from
interface states, we plot the conductance peak value as a function of reciprocal temperature in Fig. 3. Very weak temperature dependencies of the conductance have been noted at 1 MHz and 50 kHz and activation energies smaller than 5 meV have been derived. An absence of activation indicates that deep defects have a negligible contribution in the charging and discharging processes in nc-Si dots (refer to a typical defect thermal activation energy: 50 ∼ 200 meV [19]). Thus, it can be concluded that in the present case the device performance depends only on the sandwiched nc-Si dots between SiO$_2$ layers.

Figure 3 The plot of the conductance peak value ($G_m$) as a function of reciprocal temperature ($1/T$) at (a) 1 MHz and (b) 50 kHz. The calculated activation energies are (a) 4.8 meV and (b) 2.3 meV.

Based on these understanding, a plausible background-charge-free MOSFET single/few electron(s) memory, shown in Fig. 4, is proposed and thoroughly investigated.

![Fig. 3 The plot of the conductance peak value ($G_m$) as a function of reciprocal temperature ($1/T$) at (a) 1 MHz and (b) 50 kHz. The calculated activation energies are (a) 4.8 meV and (b) 2.3 meV.](image)

![Fig. 4, (a) The structure schematic of the device; (b) SEM image of short and narrow channel, only 4 nc-Si dots located in this area; (c) The equivalent circuit. Three main capacitances were defined.](image)

![Fig. 5, Channel current vs. gate voltage at 77 K. The electron storing and erasing events in the floating nc-Si dot are highlighted by vertical arrows.](image)

Figure 4b shows the planer SEM image of the memory device after nc-Si dot deposition. Clearly 3–4 nc-Si dots are visible in the active region. Since the screening efficiency is strongly dependent on the separation between the dots and the width of the channel, the dots outside the narrow channel would have little effect on the device characteristics. Thus an electrical response of the device owing to trapping of charges may be attributed to that arising from the nc-Si dots only.

Figure 5 shows the variation of the channel current as a function of applied gate voltage for a typical device measured at 77 K showing a clockwise hysteresis loop with a discrete voltage shift ($V_{th}$) that is characteristic of a memory operation. Neither any hysteresis nor discrete voltages were observed in the control samples without nc-Si deposition. However, before discussing the striking features of Fig. 5, it is important to point out that the contribution from deep defects or interface states can be ruled out on the basis of results obtained with capacitor memory. Thus it is reasonable to conclude that the injected electrons delocalize over the entire nc-Si dot and stored electrons induce such $V_{th}$.

It is worth pointing out the interesting features of Fig. 5. As the gate voltage is swept forward and backward between -5 and 1 V (scan-A), a clear current drop in the $I$–$V$ characteristic around -0.08 V is observed only in forward scan, which could be considered as a direct evidence of electron trapping in the nc-Si dot at a writing voltage of 1 V. When the writing voltage is raised from 1 to 5 V and the measurement is repeated (scan-B), a drop in the channel current at a similar position with respect to the previous one appeared in the corresponding forward scan. For simplicity, discussions are restricted with writing voltages of 1 and 5 V only. Referring to Fig. 5, notable is
the appearance of an additional current jump at around -0.64 V during the backward scans from 5 to -5 V, which may be associated with the electron emission from the nc-Si dot. On the other hand, the absence of such a feature in channel current during backward sweep of the voltage in scan-A apparently suggests that the stored electron is not erased around such voltage from the nc-Si dot unlike that observed by Hinds et al. [10]. Moreover, it interesting to point out, (1) the backward $I-V$ curve of scan-A coincides with forward at and beyond one electron trapping; (2) the backward $I-V$ curve of scan-B coincides with that backward of scan-A at and beyond one electron erasing; and (2) the $V_{th}$ corresponding to the writing voltage of 5 V is found to be nearly two times as that when written at 1 V.

Summarily, in Fig. 5, the same trap voltage, the identifications of $I-V$ curves in scan-A as well as scan-B and quantitatively equal threshold voltage shift for each of electron trapping in the forward and the backward scan of both writing voltages are remarkable. These characteristics imply that the sequential charging and discharging memory operation may be from the same nc-Si dot located in the active region. Moreover, The reproducible small current steps indicated by vertical broken arrows in the scan-B are likely due to discharging of nc-Si dots nearest to the active region. Clearly, they have little influence on the overall device performance. Thus the random distribution of nc-Si dots is plausible not to be serious for the memory operations in our present devices.

The shift in the threshold voltage to the positive direction, caused by storing one of the electrons in the floating gate in our case nc-Si dot of a memory device is given by [4]

$$\Delta V_{th} = \frac{n e}{C_{fg} + C_{gc} \cdot \frac{C_{c}}{C_{fc}}}$$

(2)

$$C_{c} = C_{fg} + C_{fc}$$

(3)

where $n$ is the number of trapped electrons, $C_{fg}$ is the capacitance between floating dot and the gate, $C_{fc}$ is the capacitance between floating dot and the screened channel, and $C_{cg}$ is the capacitance between the screened channel and gate, respectively. In our device as shown in Fig. 4(c), the values of the capacitance can be estimated as $C_{fg}$ is 0.87 aF, $C_{fc}$ is 0.37 aF, and $C_{cg}$ is 0.28 aF. The calculated $V_{th}$ was 95 mV for $n = 1$, which is consistent with the experiment ~92 mV for scan-A. The $V_{th}$ of about 190 mV for scan-B indicates storing of two electrons in the nc-Si dot at a writing voltage of 5 V within errors.

A time dependent monitoring of the channel current provides a direct measure of the retention time as well as the memory state of the device. Fig. 6a and 6b depict the discharging history of the memory device under investigation at 77 K after the stress of 1 and 5 V, respectively, and read at ~0.46 V. Clearly we find no current jump of the channel current in Fig. 6a in each typical periods (60 s), which can be associated with the emission of electrons from the nc-Si dot. On the other hand, just one discrete step with a time period of about 40 s is observed in Fig. 6b. Considering the fact that each current jump corresponds to the emission of each electron, one can conclude one of the two electrons from the nc-Si dot, a retention time ~ 40 s, was erased.

![Time dependence of the channel current](image)

Fig. 6, Time dependence of the channel current after writing at (a) 1 V and (b) 5 V, respectively. Read-voltage is fixed at ~0.46 V. The measurement periods are (a) 70 s and (b) 40 s respectively. The insert is the measurement voltage function.

So far, our nc-Si dots based capacitor memory investigations suggest that the electron trapped in the dot would be delocalized in the entire dot itself. Hinds et al. reported that for such a system an nc-Si dot showed a polarization effect under a positive gate voltage, where the electron will be attracted to the top of the dot reducing the transparency [10]. It is likely that the polarization effect along with the suppressed thermal excitation at 77 K enhances the retention time of the electron stored in the nc-Si dot. However, when the second electron is stored in the same dot, the equilibrium is destabilized due to strong superposition of
electron wave functions giving rise to an electron–electron repulsive interaction. This results in the loss of one of the electrons to restore stability [20]. Therefore, one erasing process is exhibited in scan-B, but not in scan-A. A stability of multi-electron trapped few electron memory may be an interesting issue that would enable us know the very retention mechanism in further detail.

IV. Conclusion

SiO$_2$/nc-Si/SiO$_2$ sandwich structure memory devices were prepared. Sensitive electrical measurements of C-V and G-V were utilized to investigate charging and discharging in nc-Si dots. Experiments showed that neither interface defect nor deep defect was dominant for the corresponding charging and discharging processes. Operation of a MOSFET memory device based on the nc-Si dot at 77 K has been discussed in light of two different writing voltages. Although more than one nc-Si dot is statistically present in short and narrow channels of the device, it is found that only one dot determines its memory state where a threshold voltage shift of 92 mV corresponds to the trapping of one electron in the nc-Si dot. In our device the one electron memory state is found to be more stable than the two-electron memory at 77 K.

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Reference