Epitaxial Growth of Strained Si$_{1-y}$C$_y$ on Si and Its Application to MOSFET

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We succeeded to obtain Si$_{1-y}$C$_y$ films by low-temperature Si epitaxy methods, such as Hot Wire Cell method, plasma-CVD, photo-CVD and gas-source molecular beam epitaxy (GSMBE). In the work, first of all, we investigated the thermal stability of strained Si$_{1-y}$C$_y$ films grown by plasma-CVD. It was found that an annealing over 900℃ caused a formation of 3C-SiC and a relaxation of the strain. A simulation taking into account chemical reactions of defect complexes in Si$_{1-y}$C$_y$ films well explained this annealing behavior and the thermal stability of films. From this result, we found that the process temperature should be lower than 800℃. The low temperature MOSFET process in which all process temperatures after deposition of Si$_{1-y}$C$_y$ were lower than 800℃ was developed. A strained Si$_{1-y}$C$_y$ MOSFET in which channel layer was grown by Hot Wire Cell method was fabricated and characterized.

1. Introduction

Recently, group IV alloys such as Si$_{1-x-y}$Ge$_x$C$_y$ and Si$_{1-y}$C$_y$ have attracted great attention as new materials for introducing band gap engineering in the present Si technology. Furthermore, the challenge of improving device performance is carried out by the enhancement of transport properties in a MOS channel using strained Si/Si$_{1-x}$Ge$_x$ structure [1]. When the strain is introduced to the MOS channel, an effective mass of carriers would be decreased, which resulted in the increase of carrier mobility. We focused on the strained Si$_{1-y}$C$_y$/Si structure since it has several advantages, compared to using Si$_{1-x}$Ge$_x$: we can select many kinds of hydrocarbon gas as a C source for epitaxy of Si$_{1-y}$C$_y$ and they are not toxic, while GeH$_4$ is toxic. Furthermore, the thermal conductivity of Si$_{1-x}$Ge$_x$ is inferior to that of Si [2]. In our previous works, we have reported that Si$_{1-y}$C$_y$ films with a substitutional C (C$_s$) concentration of about 1% and 3% were successfully grown at 200℃ by using a Hot Wire (HW) Cell method [3] and plasma-CVD [4], respectively. However, for the MOS device processing such as oxidation, the stability of the Si$_{1-y}$C$_y$ films against the thermal treatment is very important. So, in this work, we investigated the thermal stability of Si$_{1-y}$C$_y$ films grown by plasma-CVD and the electrical property of an oxide formed by oxidizing Si$_{1-y}$C$_y$ film grown by the Hot Wire Cell method was studied. Based on these results, we applied the strained Si$_{1-y}$C$_y$/Si structure to MOSFET.

2. Experiment

For the growth of Si$_{1-y}$C$_y$ films we used RF plasma-CVD for the study of thermal stability of films and the HW Cell method for the fabrication of MOSFET. In plasma-CVD, a gas mixture of SiH$_4$ and H$_2$ was used and C$_2$H$_2$ and SiH$_4$(CH$_3$) were used as a carbon source gas. The details of plasma-CVD system were described in the reference [4]. In the HW Cell method, a tungsten filament, coiled with a diameter of 4 mm and length of 1.5 cm, was arranged lengthwise with respect to the gas inlet. This was the significant difference of our HW Cell method from other HW-CVD works [5-8]. Because of our filament layout, the reactant gas was decomposed efficiently and atomic hydrogen could be supplied to improve the crystallinity of Si films. The distance between the filament and the substrate was about 6 cm. The filament temperature was maintained at 1650-1750℃. For the growth of Si$_{1-y}$C$_y$ films, C$_2$H$_2$ gas (He: 90%, C$_2$H$_2$: 10%) was used as C source and hydrogen was also used for dilution. The details of the growth conditions for the HW Cell method were shown in the reference [3].

The crystallinity of films was confirmed by in-situ Reflection High Energy Electron Diffraction (RHEED) observation. The concentration of a substitutional carbon in the film was evaluated by a
high resolution X-ray diffractometer (HRXRD). For the MOSFET, the p-type Si substrates with a carrier concentration of $1 \times 10^{16} \text{cm}^{-3}$ was used.

3. Results and Discussions

3.1 Thermal stability of $\text{Si}_{1-y}\text{C}_y$ films

In order to investigate the thermal stability of $\text{Si}_{1-y}\text{C}_y$ films, we used films grown by plasma-CVD. Figure 1 shows the dependence of XRD (004) pattern on the annealing temperature for an epitaxial film grown at a $\text{C}_2\text{H}_2/\text{SiH}_4$ ratio of 0.005. The annealing time was 30 min. An additional XRD measurement of the asymmetric (115) reflection revealed that the film was pseudomorphically grown on the Si substrate. As can be seen in this figure, the $\text{Si}_{1-y}\text{C}_y$ film grown at a low temperature showed various behaviors on annealing temperatures. In the XRD pattern of the as-grown sample, the reflection peak of the epitaxial layer appears at the lower degree compared with that of the Si substrate. This means that the lattice of the as-grown film was expanded. This is due to an incorporation of H atoms in the Si-Si and Si-C bond centers [9, 10].

The peak shifts to the higher degree with increasing annealing temperature up to 700°C because of H desorption and we confirmed the epitaxial growth of strained $\text{Si}_{1-y}\text{C}_y$ on Si. By further annealing at higher temperatures up to 900°C, the peak position shifts again toward the Si substrate due to the formation of 3C-SiC. The formation of 3C-SiC was also confirmed by the FT-IR observations.

In order to analyze the annealing behavior of H and C atoms in the $\text{Si}_{1-y}\text{C}_y$ film, we considered that the following complexes were formed in the $\text{Si}_{1-y}\text{C}_y$ film during the annealing: H atoms locate at Si-Si bond center and at Si-C bond center, C atoms adjoining H atoms and at substitutional sites, and SiC precipitates. By assuming the chemical reactions of each complex, we can derive differential equations on the time evolutions and calculate both the concentration of each complex and the lattice constant of annealed $\text{Si}_{1-y}\text{C}_y$ films.

Figure 2 shows a variation of XRD peak angle as a function of annealing time at several annealing temperatures. Experimental results are also shown in the figure. The sample was grown using $\text{SiH}_2(\text{CH}_3)_2$. The calculated results show excellent agreements with the experimental results. Additionally, the C$_s$ stability as a functions of the initial C$_s$ composition and the annealing temperature was analyzed using the model. The result is summarized in Fig. 3. The contour lines in the figure indicate the time at which 0.1% 3C-SiC precipitates are formed by the annealing.
the Si$_{1-y}$C$_y$ alloy with $y=0.01$, the 0.1% loss of C$_s$ occurs at an annealing temperature of 800°C with a duration of 35 min, while the duration drastically decreases down to 100 sec at the temperature of 900°C. Furthermore, for the Si$_{1-y}$C$_y$ alloy with $y=0.03$, the rate of the formation of precipitates is one order of magnitude faster than that of Si$_{0.99}$C$_{0.01}$. Namely, this model showed that the loss rate of C$_s$ at the high temperature increased with increasing initial C$_s$ content in the Si$_{1-y}$C$_y$ film. This is due to that the higher C content leads to the higher encounter probability of two C atoms.

3.2 MOSFET with a strained Si$_{1-y}$C$_y$ channel

Based on the above result, we developed the fabrication process for MOSFET with a strained Si$_{1-y}$C$_y$ channel. First of all, we investigated the oxidation of Si$_{1-y}$C$_y$ films in order to investigate the influence of these precipitates in oxide films. Figure 4 shows the dependence of C$_s$ and leak current density of oxide films on annealing temperature. The samples were grown by HW Cell method at 200°C and annealed at 700°C for 30 min in N$_2$ atmosphere to desolve hydrogen. The initial C$_s$ was 0.57%. Then, they were annealed at 800, 850 and 900°C for 1 hour in N$_2$ atmosphere, followed by the wet oxidation at 800°C for 10 minutes. The thickness of oxide was about 20 nm. The C$_s$ decreased from 0.57% to 0.50% by annealing at 850°C and to 0.15% at 900°C. We found the leak current through the oxide increased by increasing the annealing temperature, suggesting that 3C-SiC precipitate or the interstitial carbon worked as defects in the Si$_{1-y}$C$_y$ oxide films. From this result, we obtained the oxide film with the leak current density of $10^{-9}$ A/cm$^2$, which is sufficient for the study of MOSFET.

We applied the strained Si$_{1-y}$C$_y$ films to MOSFET channel. By using tensilely strained Si$_{1-y}$C$_y$ as a channel, the enhancement of device performance could be expected due to the reduction of effective electron mass [11, 12]. In the study of thermal stability of Si$_{1-y}$C$_y$ films, we have found that the process temperature for device fabrications should be lower than 800°C. In order to avoid the thermal treatment to Si$_{1-y}$C$_y$ at high temperature, source and drain regions were firstly fabricated by thermal
diffusion of phosphorus at 900°C. After that, the Si$_{1-y}$C$_y$ films (N$_D$ $\equiv$ 1x10$^{17}$ cm$^{-3}$) were grown by HW Cell method at the gate region. The thickness of the epitaxial Si$_{1-y}$C$_y$ films was 50 nm. The amorphous Si$_{1-y}$C$_y$ film grown on other region (SiO$_2$) was etched by CF$_4$ plasma. Then, annealing at 800°C was carried out in N$_2$ atmosphere for 30 min to dissolve the hydrogen from the grown films. The gate oxide was grown by wet oxidation at 800°C for 10 minutes, followed by dry oxidation for 5 minutes to improve the quality of SiO$_2$. Al was evaporated as an electrode. Also the post metallization annealing was carried out at 450°C for 30 minutes in forming gas (N$_2$: 95%, H$_2$: 5%) atmosphere. The gate length was designed as 5 and 10 µm and the gate width was 20 µm.

The $I_D$-$V_D$ characteristics of strained Si$_{1-y}$C$_y$/Si channel MOSFET are shown in Figures 5 (a) C$_s$=0%, upper figure and (b) C$_s$=0.78%, lower figure. In both characteristics, the dependence on the gate voltage was observed and we found the operation of Si$_{1-y}$C$_y$/Si MOSFET with the low temperature process. However, the initial rise of $I_D$ around $V_D$=-0.2V was not steep. This suggested the existence of some barrier such as oxide or other contaminants at the interface between Si and Si$_{1-y}$C$_y$. The effective electron mobility was calculated from the linear region of $I_D$-$V_D$ characteristics. Figure 6 shows the dependence of relative effective mobility (based on the mobility with C$_s$=0%) on C$_s$. It decreased by 18% from the sample with C$_s$=0% to that with C$_s$=0.78%. This slight decrease of mobility was mainly caused by the degradation of film quality due to poor interface between Si$_{1-y}$C$_y$ and Si substrate.

3. Conclusions

We investigated the thermal stability of strained Si$_{1-y}$C$_y$ films. Annealing over 900°C caused the formation of 3C-SiC and the relaxation of the strain occurred. We also fabricated the MOS structure and found that leak current through Si$_{1-y}$C$_y$ oxide increased by increasing annealing temperature. From this result, we found that the process temperature should be lower than 800°C for the strained Si$_{1-y}$C$_y$ films. The low temperature process to apply Si$_{1-y}$C$_y$ films as MOSFET channel. The Si$_{1-y}$C$_y$ films were grown on the gate region, followed by thermal oxidation at 800°C. The $I_D$-$V_D$ characteristics were measured and the effective mobility was evaluated.

4. Reference