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QNERC
Quantum Nanoelectronics Research Center

QNERC NEWS

Practical Guidance from a Pioneer in Building Nanostructures

Klaus Ploog
Visiting Professor

"The people at Tokyo Tech understand what is necessary for productive research in nanotechnology," declares visiting professor Dr. Klaus Ploog. "And they have equipped this center to support world-class work in that field."

Ploog has worked extensively in private-sector industry, as well as in public-sector research and academia. He built his formidable reputation partly by demonstrating uncanny skill and creativity in using molecular beam epitaxy to fashion crystals from individual atoms. Ploog ranks among the German scientists most frequently cited in scientific papers published worldwide. The German government named him to head the newly established Paul Drude Institute for Solid State Electronics in Berlin in 1992. And he retains a relationship with that institute as a professor emeritus since 2006.

Promoting international collaboration

As director of the Paul Drude Institute, Ploog was highly active in promoting scientific exchange between Germany and Japan, especially in regard to semiconductors. He served as honorary head of the scientific working group at Berlin's Japanese-German Center, and he has organized several joint projects between researchers in the two nations. His ties with Tokyo Tech span three decades.

Ploog was a pioneer in employing molecular beam epitaxy to deposit crystals on other crystals of very different lattice measurements; for example, manganese arsenide or iron atop gallium arsenide. The resultant, monolithically integrated units can support new or improved functionality in information technology. They can even contain biologically active substances. Work by Ploog and his colleagues in self-organizing nanostructure epitaxy has yielded especially interesting results, and he continues to promote that work through international collaborations.

"A practical perspective based on working experience in industry is absolutely essential to leading-edge research," Ploog emphasizes. "Tokyo Tech's Quantum Nanoelectronics Research Center maintains excellent ties with industry, and I am confident that those ties will become stronger still."

Dr. Ploog has led important advances in using molecular beam epitaxy to achieve new kinds of functionality in semiconductor devices.

The Tokyo Institute of Technology (Tokyo Tech), Japan's foremost university devoted to technological disciplines, established QNERC in April 2004. QNERC inherits the R&D portfolio of its predecessor, Tokyo Tech's Research Center for Quantum Effect Electronics. It translates advances in nanoscience into practical suggestions for industrial applications.

Finding real-world solutions

GaInAsP/InP membrane buried-heterostructure distributed-feedback lasers directly bonded on silicon-on-insulator substrate

A membrane laser allows for increasing optical confinement in the active layer because of the large refractive-index difference between the active layer and the cladding layers. A membrane distributed-feedback (DFB) laser, consisting of deeply etched single-quantum-well wirelike active regions, can be used to fabricate ultracompact optical circuits at the low-loss fiber communication wavelength in the integration of functional photonic devices.

Shigehisa Arai and colleagues have built and operated a buried–heterostructure (BH) membrane DFB laser directly bonded on a silicon-on-insulator (SOI) substrate. To maintain a high coupling coefficient between the membrane laser and the silicon waveguide, they used a silicon thickness of 60 nm, which ensured a 70% coupling coefficient. This thin silicon layer, on 2 μm-thick SiO_2, served as the initial substrate, which was rendered hydrophilic by H_2SO_4:H_2O_2:H_2O at room temperature. Then, GaInAsP/InP and the SOI substrate were affixed to each other under pressure and annealed in an H2 atmosphere at 450°C for 60 minutes. Finally, selective wet etching was carried out to leave a thin active layer on the SOI substrate.

A smooth interface between the GaInAsP membrane layer and the SOI was observed. Room-temperature continuous-wave (RT-CW) operation has been demonstrated with single-mode oscillation at 1,579 nm with a threshold power of 2.8 mW (threshold current: 26 μA) with a stripe width of 2 μm and a cavity length of 120 μm.

This device can be applied to the integration of III-V light sources on high-density passive SOI photonic integrated circuits. A low threshold operation in the membrane laser is expected with a surface corrugation structure. A threshold power of 0.34 mW (the corresponding threshold current is 24 μA) has been obtained with a benzocyclobutene-cladding membrane DFB laser.

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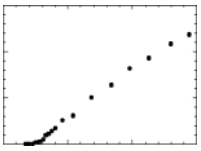

Light output characteristic of membrane DFB laser under RT-CW conditions

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Fabrication of low threshold current density GaInAsP/InP quantum-wire distributed feedback lasers with a low-damage process

High-performance semiconductor lasers offer low threshold current density in optical communications systems. Quantum-wire (Q-Wire) lasers are promising in regard to low threshold current operation, high quantum efficiency, and narrow line width.

Shigehisa Arai and colleagues had achieved low damage at the etched/regrown interfaces of the Q-Wire active regions fabricated by EB lithography, dry etching, and two-step organometallic vapor phase epitaxial regrowth. The GaInAsP/InP Q-Wire laser (wire-width [W] of 23 nm with a period [Λ] of 80 nm) provided reliable RT-CW operation without serious performance degradation, even after 32,000 hours. Using a high mesa stripe formed by deep dry etching, threshold current (2.7 mA) RT-CW operation was achieved with GaInAsP/InP lasers that consisted of Q-Wire distributed feedback (DFB) active regions (W = 24nm, Λ = 240nm). Nonradiative recombination at the sidewalls of the high mesa stripe increases the threshold current density.

Wet-chemical etching was used instead of the deep dry etching method to form a high mesa stripe. The nonradiative recombination was evaluated as the product of the nonradiative recombination velocity and the carrier lifetime ($S{\cdot}\tau$). The $S{\cdot}\tau$ product of the stripe fabricated by wet-chemical etching declined 78%, to 181 nm, from 818 nm, and the threshold current density (J_{th}) declined 35%, to 176 A/cm², from 270 A/cm². Those improvements suggest progress in developing high-performance semiconductor lasers for optical communications systems.

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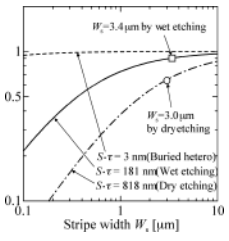

Stripe-width dependences of relative spontaneous emission efficiency

Improving the efficiency of the Hall effect micro-biosensor platform

Biosensing technology has reached the stage where biorecognition reactions are well established and a range of commercial detection methods exists. Biosensors that use superparamagnetic beads, such as the Hall effect micro-biosensor platform, exhibit distinctive advantages and commercial potential. Fulfilling that potential will depend, however, on improvements in the time and cost efficiency of the proposed techniques.

Adarsh Sandhu and his colleagues and students demonstrate an approach that greatly reduces the time required for immobilizing the magnetic labels on the sensor surface and that minimizes the amount of expensive reagent used as the functionalized superparamagnetic beads in the analytical process. They incorporate, inside the multilayered structure of the sensor, gold microlines that conduct electric currents of 1 mA to 10 mA and that generate a precisely localized electromagnetic field.

The sharp gradients of the magnetic field produce sufficient forces to attract magnetized beads to the area intended for immobilization. This process allows for attaining the required concentration of beads in the sensor area in less time than has been possible with other methods and with less consumption of reagent. It thus improves greatly the overall efficiency of the Hall effect micro-biosensor platform.

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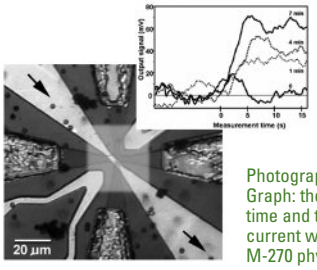
Biosensors and Bioelectronics (2006), doi:10.1016/j.bios.2006.09.021 (in press).



Photograph: a 5×5 μm² AlGaAs/InGaAs integrated sensor
Graph: the Hall voltage as a function of measurement time and the background monitored before the Hall current was applied (t = 0 s); results for Dynabeads M-270 physically adsorbed

Nanoelectromechanical nonvolatile memory device incorporating nanocrystalline Si dots

High-speed programmable/erasable nonvolatile semiconductor memory devices are desirable for improving nonvolatile memory applications in mobile products and also as a substitute for embedded memory applications. Most memories developed recently require the introduction of an unconventional material in the silicon device fabrication processes. Achieving an alternative bistability mechanism entirely with conventional silicon-based materials would simplify those processes.

Yoshishige Tsuchiya and colleagues from Tokyo Tech and Hitachi Ltd. have proposed a new-concept nanoelectromechanical nonvolatile memory device that uses nanocrystalline silicon (nc-Si) dots. They used the mechanical bistability of a floating gate where the nc-Si dots were embedded as charge storage. The operational speed of electromechanical systems increases with decreasing size, so extremely fast operation appears possible. The proposed device also offers an advantage in regard to future integration with advanced silicon circuits because it allows for fabrication with conventional silicon technology.

Superior on-off characteristics are demonstrated by using an equivalent circuit model that accommodates the variable capacitance that results from the mechanical displacement of the floating gate. Mechanical property analysis conducted with the finite element method shows that the introduction of an nc-Si dot array into the movable floating gate results in a reduction in switching power. High switching frequency of more than 1 GHz is achieved by decreasing the length of the floating gate to the submicron range. Experiments confirmed the mechanical bistability of the SiO_2 beam fabricated with conventional silicon etching processes.

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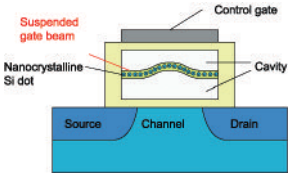

A schematic diagram of a nanoelectromechanical nonvolatile memory device that incorporates nanocrystalline-Si dots

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High temperature scanning Hall probe microscopy (HT-SHPM) using AlGaN/GaN 2DEG micro-Hall probes

Scanning Hall probe microscopy (HT-SHPM) is a well-established commercial technique for monitoring localized magnetic field fluctuations, with or without an external magnetic field applied. It offers important advantages, such as noninvasive measurement, reliable quantification, and operability across a wide temperature range. Expanding the applicability of scanning Hall probe microscopy will depend on progress in broadening the operable temperature range further and in improving electronic and physical stability.

Primadani, Osawa, and Sandhu demonstrate the application of AlGaN/GaN heterostructures that feature two-dimensional electron gas (2DEG) as new micro-Hall probes for scanning Hall probe microscopic measurements at elevated temperature, with an external magnetic field applied. AlGaN/GaN heterostructures offer advantages as wide-bandgap (2.5 eV or greater) semiconductors, where the probability of thermally induced electron excitation in the conduction band is reduced and where the presence of the 2DEG layer ensures high electron mobility and high probe sensitivity.

The fabricated $2 \times 2\ \mu m^2$ probes exhibit a Hall coefficient of 0.01 Ω/G and a magnetic field sensitivity of 8.3 mG/Hz$^{1/2}$, and they were effective in observing magnetic domains in garnet films at temperatures of up to 100°C. Further improvements envisioned by the authors could extend the operable temperature upward, to 500°C, which would greatly increase the range of commercial applications.

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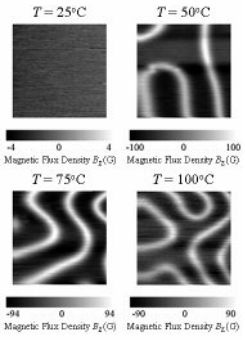
Japanese Journal of Applied Physics (2007, in press).



Scanning Hall probe microscopic images of a 50 μm x 50 μm area of a garnet film under an external perpendicular magnetic field of 150 Oe and at varied temperature

A new design concept and fabrication process for three-dimensional silicon photonic crystal structures

Three-dimensional photonic crystals (3DPCs) are a promising means of controlling light by inhibiting the propagation of all optical modes within the photonic band gap. Recently, considerable effort has been invested in the fabrication of 3DPCs. Downscaling and increasing the number of layers are crucial in optimizing performance in individual fabrication processes, but in most of those processes, increasing the number of layers causes problems in alignment between layers, especially in the small spectral range centered at around 1 μm.

Daihei Hippo and colleagues from Tokyo Tech and the Tokyo University of Agriculture and Technology have used two directional electrochemical etching processes in a magnetic field to create 3DPC structures on 100 nm scale. The fabrication processes consist of three fundamental techniques: (a) the first directional etching from the top surface, (b) mechanical polishing on the slope, and (c) the second directional etching, perpendicular to the first directional etching and in conformance with a pattern formed on the slope as a guide (fig. 1).

Hippo and his colleagues observed the formation of two-dimensional periodic pores 80 nm in diameter and aspect ratios of greater than 80 on the n^+ (100) silicon substrate. They also observed a clear directionality in the pore formation in two directions, which suggests the possibility of projecting the slope pattern on the side of the wafer (fig. 2). These fundamental etching processes are applicable to the fabrication of the 3DPCs in the visible range without resorting to any alignment processes.

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Fig. 1. A schematic of the proposed fabrication process

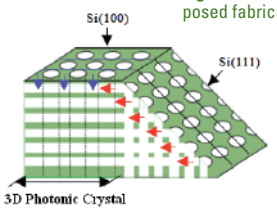
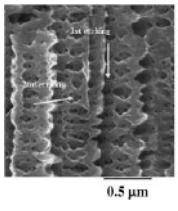


Fig. 2. Fabricated 3DPC on 100 nm scale



Finding real-world solutions

Growing strain-relaxed $Si_{1-y}C_y$ films with silicon-on-insulator substrates

Strain-induced mobility enhancement is a widely used technique in creating high-speed Si MOSFETs. However, the commonly used $Si/Si_{1-x}Ge_x$ system enhances mobility only in a horizontal plane; it does not allow for enhancing mobility vertically.

Akira Yamada and colleagues have developed a strain-relaxed $Si_{1-y}C_y/Si$ system that uses silicon-on-insulator (SOI) substrates, and they have employed the system as a buffer layer for tensilely strained Si. The tensilely strained Si is applicable to vertical MOSFETs.

$Si_{1-y}C_y$ films were grown with gas-source molecular beam epitaxy (GS-MBE) using a gas mixture of Si_2H_6 and C_2H_2 on a SOI substrate whose Si layer was 30 nm thick. The thin Si layer, which is on a buried-oxide layer, acts as a sink of dislocations and improves the film qualities of the $Si_{1-y}C_y$ layers. The next aims of the project are to grow tensilely strained Si on the high-quality strain-relaxed $Si_{1-y}C_y$ buffer layers and to apply the strained layer to vertical MOSFETs, whose principal advantage is controllability of the channel width.

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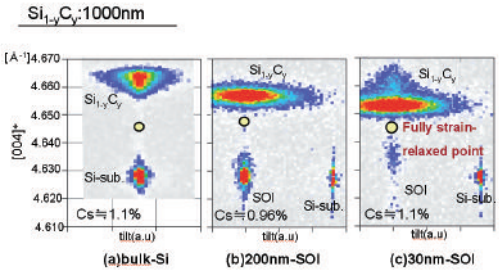
Journal of Crystal Growth (2007, in press).



Reciprocal space maps of strain-relaxed $Si_{1-y}C_y$ layers grown on (a) bulk-Si, (b) 200 nm SOI, and (c) 30 nm SOI around (004) the reciprocal lattice point; the carbon content (Cs) of the layers is about 1.0%

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Fabrication and characterization of strained $Si_{1-y}C_y$ n-MOSFETs grown by the hot wire cell method

A $Si_{1-x}Ge_x$ layer grown on a Si substrate is used as a buffer layer in strained Si technologies. However, the thermal conductivity of $Si_{1-x}Ge_x$ is poor compared with that of Si and $Si_{1-y}C_y$, and that causes heat generation during device operation.

Akira Yamada and colleagues have focused on compressively strained $Si_{1-y}C_y/Si$ structure as an alternative to compressively strained $Si/Si_{1-x}Ge_x$ structure. The compressively strained $Si_{1-y}C_y$ layer in the subject of their research acts as a channel of n-MOSFETs. The merit of the structure is high thermal conductivity, compared with $Si_{1-x}Ge_x$.

Strained $Si_{1-y}C_y$ layers were grown on a Si substrate at a temperature of 200˚C with the hot wire cell method. The low growth temperature was crucial in growing the $Si_{1-y}C_y$ layers with a carbon content (Cs) up to 1% because carbon atoms are prone to segregate in the silicon matrix at high temperatures. The layers were applied to the channel of n-MOSFETs.

The drain current of the devices revealed the improvement that resulted from the addition of carbon. The improvement of the effective mobility was demonstrated by introducing stress into the channel.

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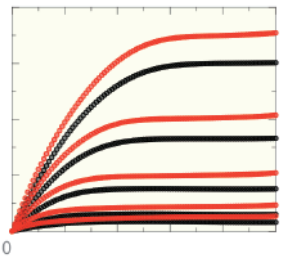

Drain current-drain voltage characteristics of $Si_{1-y}C_y$ MOSFET, where the solid line indicates the result for Cs = 0.78% and the dashed line the result for Cs = 0%

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