Ballistic transport in Si vertical transistors

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Abstract

Vertical silicon transistors with a wrap gate are shown to exhibit quantum ballistic transport. The vertical design readily allows smaller channel length with reduced scattering sites. In DC measurement, the conductance characteristics show quantized plateaus at multiples of $4e^2/h$ at 5K. Under magnetic field, the conductance is reduced by 1/2 and 1/4. This effect is likely the result of spin and valley splitting. The transport characteristics are investigated for various geometry of the point contact.

Ⅰ. Introduction

In recent years, the size of semiconductor devices has been reduced dramatically. According to The international Semiconductor Technology Roadmap, this trend will continue until 2012, when the minimum feature size of 50nm is projected. However, further reduction is difficult due to several problems, including fabrication technique and the short channel effect. Moreover the mesoscopic effect occurs in nanoscale MOS transistors. When the devices become smaller than the electron mean free path, electrons travel through the active region without scattering and must be treated with Landauer formalism. In this regime, devices without electron fluctuation obtain high current drivability. By using high-mobility two-dimensional (2D) electron gas and split gate structures formed in a $GaAs/Al_xGa_{1-x}As$ heterojunction, van Wees *et al*[1] fabricated quantum point contacts (QPC) with smaller length and width of the channel than the phase-preserving length and comparable with Fermi wavelength. They observed that the two-terminal conductance of the QPC was quantized in units of $2e^2/h$ as a function of the width constriction. Other researchers[2-4] also investigated the conductance quantization in 1D systems using metals and semiconductors. However, there are only a few reports on the conductance quantization in silicon,[5-8] due to the lower mobility, the shorter phase-coherence length, and shorter elastic and inelastic mean free path of Si. Thus the investigation of the conductance quantization with the Si QPC needs the smaller structure than the case of metals and compound semiconductors.

In this work, we have fabricated a nano-meter scale vertical-structure silicon FET with a wrap gate by electron beam lithography and the chemical vapor deposition (CVD). The width and length of the channel is smaller than the elastic electron mean free path in silicon, thus we can observe the conductance quantization. We investigate the conductance characteristics as a function of magnetic field. From them, which allows the estimation of a device dimension and sub-bands in a silicon point contact. The shape of the device is seen to affect ballistic transport characteristics remarkably.

Ⅱ. Fabrication

Fig. 1 shows the fabrication process. The vertical-structure silicon FET was fabricated on, As-doped ($10^{18}cm^{-3}$) Si(100) wafer with a resistivity of 0.002 Ω・cm. After the standard Si wafer cleaning followed by diluted HF treatment, 20-nm-thick thermal SiO_2 layer was grown at 1000 °C. Onto this, the poly-crystalline Si (poly-Si) gate electrode was deposited. Low density of states (DOS) on the gate electrode is desirable, because the electron trapping in gate DOS results in the random telegraph signal. In order to prepare poly-Si with a large grain size and low DOS, we first deposited amorphous Si (a-Si) followed by solid-phase crystallization.[9,10] 20-nm-thick a-Si with a P doping concentration of 10^{18} cm^{-3} was deposited using Hg sensitized photo-CVD at 250 °C. For the crystallization process, the sample is first annealed at 700 °C for 4 hours in N_2, followed by at 900 °C for 1 hour. This process results in the grain size

parallel to the surface of 100-200 nm, while grain

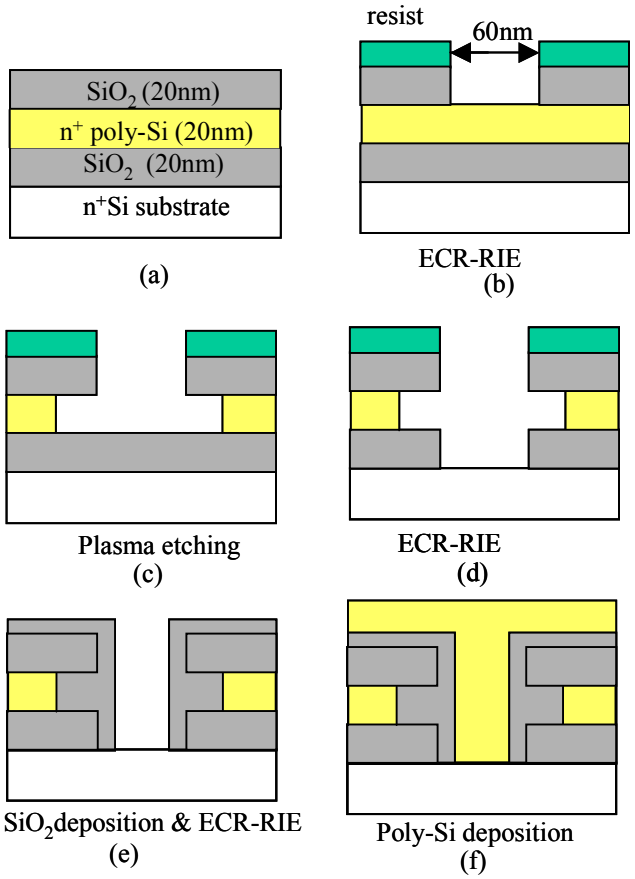

Fig.1: Fabrication processes (f) The final structure.

size perpendicular to the surface is determined by the film thickness of 20nm. A 20nm-thick SiO_2 layer was deposited with the plasma enhanced CVD using tetraethoxysilane (TEOS) followed by annealing at 1100 °C for 2 hours (Fig. 1(a)).

Then 60 nm × 60 nm holes for the top electrode were made by electron beam lithography of ZEP-520 positive resist diluted with ZEP-S (1:3). After developing the resist, the upper SiO_2 was etched completely with electron cyclotron resonance reactive ion etcing (ECR-RIE) using CF_4 etching gas because of anisotropic and selective etching of SiO_2 (Fig. 1(b)). Then the gate electrode poly-Si was etched by the direct plasma and CF_4+10% O_2 gas mixture because of isotropic and selective etching for poly-Si. The isotropic etching allows sidewall etching and controls resulting distance between the channel and the gate (Fig. 1(c)). Next the lower SiO_2 was etched by ECR-RIE (Fig. 1(d)). After these procedures, the poly-Si gate and the Si bottom electrode exposed to air are terminated by fluorine. Damages caused by etching and fluorine will adversely create DOS and affect the electric measurement. Thus 800°C-oxidation for 20 minutes was performed to remove the interface states and the oxide layer with fluoride impurity was removed with 1% HF. The sample was immersed in H_2SO_4:H_2O_2=1:1 solution at 80 °C for 10 minutes to passivate the surface with oxide. Once more a 20 nm-thick SiO_2 layer was deposited by plasma enhanced CVD of TEOS followed by annealing at 1100 °C for 2 hours. After that, SiO_2 was etched by ECR-RIE using CF_4 etching gas (Fig. 1(e)). Finally, the top electrode was made from 30 nm-thick a-Si followed by the crystallization with SPC method (Fig. 1(g)). The conformal coverage characteristic of CVD method allows the top electrode to cover the hole completely.

Ⅲ. Results and Discussions

We measured electrical transport of the sample using the two-terminal DC measurement system with temperature controlled by a helium cryostat system. The bottom electrode is grounded and the top electrode is biased. When the bias voltage V_b was varied, at gate voltage V_g=0 V, the current characteristic did not change between 3K and 10K. If a-Si is not completely crystallized or the grain boundaries of poly-Si exist in the carrier path, variable range hopping (VRH) should be observed at low temperatures. The VRH current is proportional to $\exp[-(T_0/T)^{1/4}]$, where T_0 is a characteristic constant and T is the temperature. In our case, the conductance is independent of temperature, thus a-Si is crystallized completely in the channel path.

Fig. 2 shows that the conductance changed as staircase-like characteristics with a step height of $4e^2/h$ at a low bias voltage of -1mV under various magnetic field conditions. Temperature is 5K. These characteristics are expected to result from ballistic transport. For the observation of clear ballistic transport, the channel width and length must be shorter than the electron mean free path. Hall measurement of bulk poly-Si deposited on SiO_2 indicated that the carrier concentration N_c is ~10^{13} /cm^2 and the carrier mobility μ is ~10^3 cm^2/V·s at 5 K. From these values, we obtain the values of the Fermi energy 63 meV, Fermi wavelength 11 nm, inelastic mean free path $l_{in}=\mu h(2\pi N_c)^{1/2}/2\pi e\approx$300 nm, and elastic mean free path

$l_{el}=G_s h/4\pi e^2(\pi N_c)^{1/2}\approx 45$nm, where G_s is the sheet conductance, and h is the Planck constant. It should be noted that these values are obtained from the poly-Si film, deposited on SiO_2, with the channel

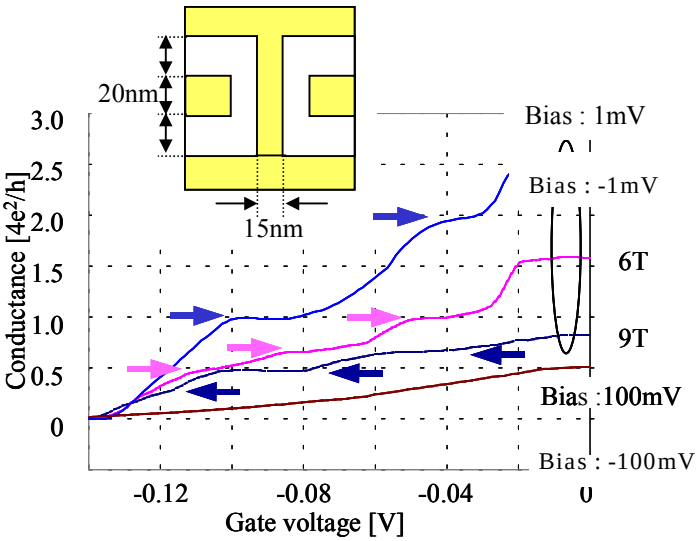

Fig. 2 Conductance characteristics as a function of a gate voltage under various magnetic field at a bias voltage of 1 mV. Temperature is 5K. For comparison, non-ballistic region case at a bias voltage of -100mV is also shown. The inset is the estimated device structure.

length longer than 200 μm. In this vertical device, the length of the channel corresponds to the thickness of the poly-Si film for the gate electrode and no grain boundary exist in the channel as a mention above. l_{in} and l_{el} of the vertical device are expected to be considerably longer than those mentioned above. However, even with the lower values, the width of the channel is narrower than the inelastic mean free path and narrower than or comparable to the elastic mean free path. And the lead connected to a small point contact is also formed by poly-Si with a large grain size. Small stray resistances enable to observe clear steps resulting from ballistic transport.

Reflection in the channel is one reason for not observing clear conductance quantization. In other reports[1,2] using compound semiconductor, the carriers are confined at the interface of heterojunctions. In that case, the carriers are affected by the interface states. This leads to increasing of the reflection, and conductance quantization becomes unclear. But in our devices, the region near the interface between SiO_2 and poly-Si is depleted by the gate potential, thus carrier path is away from and hence is not affected by interface states. Another reason for clear quantization steps is that the confinement in the high doping layer is sharper than that in lightly doped layer, leading to discrete subbands in channel. This prevents carriers from scattering between the neighboring subbands resulting in increased conductance.

As magnetic field perpendicular to the channel increases, the conductance is decreased. And a value of the quantized conductance became half or quarter. In an assumption that this decrease results from a negative magnetic resistance, which serves as a series resistance. However, this cannot completely explain observed data. At 6T, a thermal energy at 5K (0.43meV) is smaller than the difference of spin split by Zeeman effect of 0.7meV. Moreover, the condition for observation of Landau level ($B\mu>1$) is satisfied. We thus expect that the conductance decrease under magnetic field results from spin and valley splitting.

From the characteristic at a high bias voltage, we clearly observe that a ballistic transport increases a current drivability, compared to non-ballistic transport condition. We estimate the device dimension as shown in the inset of Fig. 2. From this estimation, we roughly calculate subband energy levels. Fig. 3(a) shows subband energies as a function of a channel width in an assumption of 1D quantum confinement, including energies with spin splitting at 9T. Fermi energy of leads is estimated from the characteristic under zero magnetic field. From observed characteristics at a gate voltage of 0V, less than four channels under Fermi energy exist. However, the calculated characteristics do not agree with observed one because at least eight channels under Fermi energy should exist. Next, we estimate the valley splitting. Under magnetic field, for a pair of valleys along the [100] axis, defined x-axis, the effective mass equation is

$$\left[\frac{1}{2m_l}\left(i\eta\frac{\partial}{\partial x}\pm\eta a+eBy\right)^2-\frac{\eta^2}{2m_t}\frac{\partial^2}{\partial y^2}-\frac{1}{2m_t}\eta^2\frac{\partial^2}{\partial z^2}+V(y,z)\right]\phi=\varepsilon\phi \quad , \quad (1)$$

where $m_t=0.19m_0$ is a transverse mass, $m_l=0.98m_0$ is a longitudinal mass, a is the distance of the center of the ellipsoids from the Γ point in k-space, $V(y,z)$ is cross sectional potential along x axis, B is magnetic field, ε is energy eigenstate, and ϕ is wave

function. As mentioned above, the channel is assumed to be single crystal, which is supported by the clear observation of ballistic transport. We assume that poly-Si would grow with the substrate orientation (100). Other assumptions are that the energy of channel would be flat, and that the energy of depleted region would be infinite against channel. In these assumptions, ϕ can be shown as

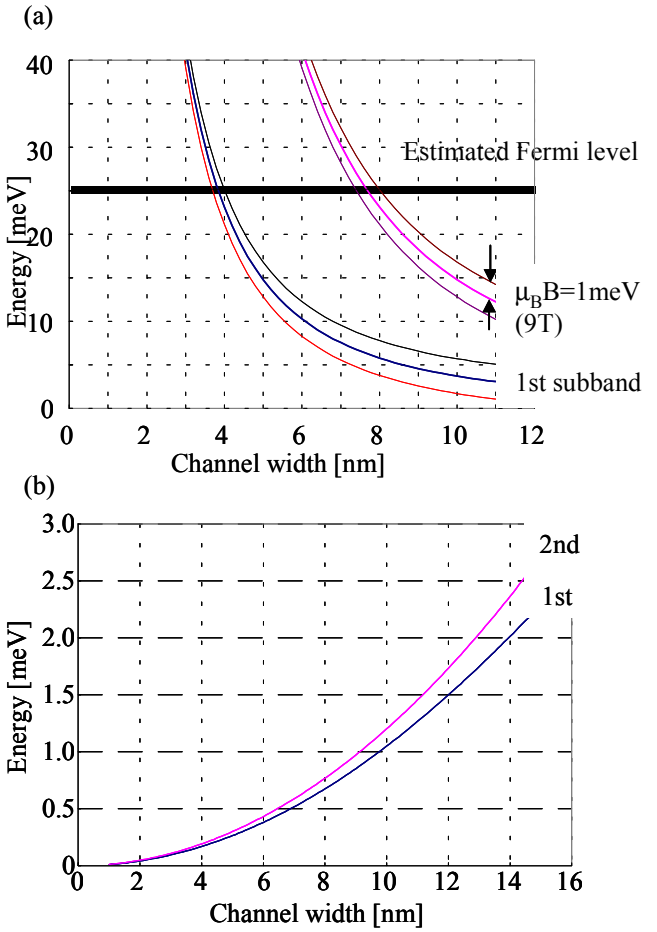

Fig. 3 (a)Calculated subband energies and spin splitting as a function of a channel width. Fermi energy is estimated from the characteristic without magnetic field.(b) Calculated valley splitting level as a function of a channel width.

$$\phi = \exp(\pm iax)\exp(ik_x x)\phi(y)\phi(z), \qquad (2)$$

where k_x is the wave number in the y direction. And, eq. (2) can transform eq. (1) to

$$\left[\frac{1}{2m_t}\left(-i\eta k_x + eBy\right)^2 - \frac{1}{2m_t}\eta^2\frac{\partial^2}{\partial y^2} + V(y)\right]\phi = \varepsilon_y\phi \qquad (3)$$

$$V(y) = \begin{cases} 0 & (|y| < d_y) \\ \infty & (|y| > d_y) \end{cases}$$

$$\left[-\frac{1}{2m_l}\eta^2\frac{\partial^2}{\partial z^2} + V(z)\right]\phi = \varepsilon_z\phi \quad V(z) = \begin{cases} 0 & (|z| < d_z) \\ \infty & (|z| > d_z) \end{cases}, \qquad (4)$$

$$\varepsilon = n^2\frac{\pi^2\eta^2}{2m_l d_z^{\,2}} + \varepsilon_y, \qquad (5)$$

where n is integer, d_y and d_z are the cross sectional size of the channel normal to the substrate. We can estimate the energy difference of valley splitting as shown in Fig. 3(b). In this case also, the splitting level is much smaller than estimated Fermi energy, thus some basic assumptions must be reexamined. Assuming a parabolic energy level would actually decrease the splitting level compared to the calculated level using square well potential. One possible reason for the observed characteristics is the negative magnetic resistance in leads connected to the point contact, which decreases the conductance. However, more investigation is required.

At a gate voltage of greater than –20mV, conductance characteristics saturate at all magnetic fields. This saturation is expected to result from a shielding effect due to density of states in the gate oxide. This explanation is supported by the fact that threshold voltage remains almost independent of the bias voltage. But in the ballistic region, at a positive gate voltage, sub-bands in the point contact are decreased relative to Fermi energy, so the conductance from higher sub-bands is expected to increase. This leads higher conductivity devices.

Ⅳ. Effect of the channel shape

We investigated the effect of the channel shape. ECR-RIE for the formation of a small trench makes the etched shape tapered at proper conditions as

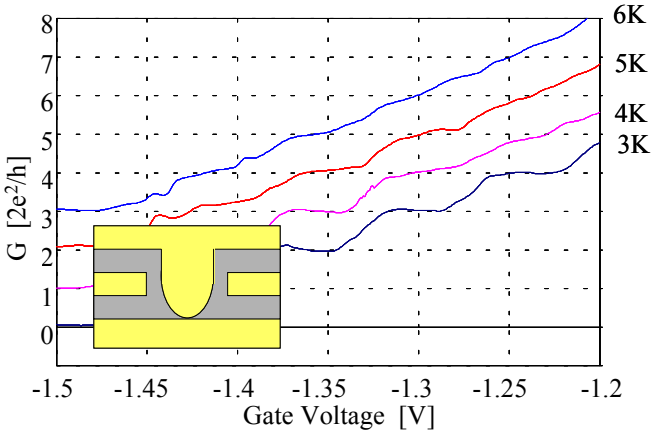

Fig. 4 Conductance characteristics as a function of a gate voltage at various temperatures in a device with the tapered. A bias voltage of -1mV. For clarity, curves are shifted vertically by $2e^2/h$. The inset is the device structure with a tapered channel .

shown in the inset of figure 4. Figure 4 shows that the current as a function of V_g at V_b=-1 mV, for various temperatures between 3K and 6K. For clarity, traces are shifted vertically by $2e^2/h$. At 3K, 4K, and 5K the conductance G is quantized to $G=N\times 2e^2/h$, where N is an integer. As the temperature increases, the conductance quantization is gradually smeared, until 6K when conductance quantization is not observed. These characteristics indicate observation of ballistic transport. However, the ideal value is $4e^2/h$, due to spin and valley degeneracy as is observed for cylindrical shaped channel. The tapered channel results in half the conductance value. Two possible explanations are that a double point contact was formed or a bias voltage was bigger than a difference of sub-band energies[11]. However, it is evident that the shape of the channel affects conductance characteristics notably. For achieving high current drivability, we must optimize the shape of channel.

Ⅴ. Conclusion

We observed, for the first time, clear quantized conductance due to ballistic transport in a silicon vertical transistor at 5K. Moreover, under magnetic field, we observed the splitting of degeneracy of spin and valley, which reinforced the ballistic transport model. This means that we have successfully prepared the smallest Si transistor with channel size much smaller than electron mean free path. In ballistic transport, we can increase a current drivability compared to conventional transistors. It is expected that the operating temperature and conductance can be increased by increasing a mean free path of carriers. An optimized shape of device is also required for the observation of ideal ballistic transport, leading to higher conductivity.

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