Fabrication of Vertical PtSi Schottky source/drain MOSFETs for Integration with Resonant Tunneling Diodes

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Abstract

We report on the dependence of the drain current on the gate oxide thickness for vertical PtSi Schottky source/drain metal oxide semiconductor field effect transistors, which are suitable devices for combining with quantum effect devices such as resonant tunneling diodes. The fabricated device structure, which has the metal gate facing toward the Schottky source, consists of a 10-nm-thick Si channel, a 5- or 8-nm-thick gate oxide and a 55-nm-long vertical channel. The drain current at V_{DS}=-1.5V and V_{GS}=-2.0V was 30μA/μm for devices in which the gate oxide was 5nm thick. This value was twenty times larger than that for devices with an 8-nm-thick gate oxide. Comparison of the drain current between the measurements and calculation showed good agreement. Based on this comparison, a drivability of about 150μA/μm can be achieved with a 3-nm-thick gate oxide.

1. Introduction

As circuits have become more and more highly integrated, a great deal of research has focused on small-geometry transistors. At geometries as small as 10nm, quantum effects exert a strong influence on the device characteristics. The application of these quantum effects to device operation has already been discussed[1,2], because quantum effect devices, such as resonant tunneling diodes (RTDs), have the potential for multi-functional operation and are inherently small in size, and both features are expected to reduce circuit complexity in highly integrated circuits.

In order to use RTDs, transistors are required to drive the circuits. We expect that vertical transistor geometry will be most suitable for combination with a resonant tunneling diode, which have the potential for multi-functional operation that are expected to reduce circuit complexity in highly integrated circuits. We proposed the use of a vertical geometry transistor, which utilizes Schottky barrier tunneling as the current source for this application. In the case of Schottky source/drain metal oxide semiconductor field effect transistors (MOSFETs), the usual implanted/diffused highly doped regions for the source and drain are replaced with silicide regions that essentially behave like metals. Several experimental structures for planar-type Schottky source/drain MOSFETs have previously been fabricated and these showed good current drivability. This device is also an attractive choice for new vertical devices combined with an RTD because it exhibits the following advantages. PtSi, which is used as a p-type silicided source and drain due to its low Schottky barrier height, has a high thermal stability, and this is required in order to grow RTDs epitaxially on a Si substrate, such as with Si/CaF_2[3,4] or CdF_2/CaF_2[5] heterostructures, which have a high peak-to-valley ratio. Furthermore, the silicided source and drain do not require annealing in order to activate the dopants. Therefore, the epitaxially grown heterostructures are free from thermal damage.

In this paper, we show the theoretical characteristics of a p-type vertical PtSi Schottky source/drain MOSFET and demonstrate devices with either 5- or 8-nm-thick gate oxide and a 10-nm-thick Si channel. The theoretical drain current in the `on' state was compared with the measurements from the viewpoint of its dependence on the gate oxide thickness.

2. Device Structure and Operation Principle

Figure 1(a) shows the schematic cross-sectional structure of a p-type vertical PtSi Schottky source/drain MOSFET. PtSi has a very low Schottky barrier height (0.24eV) for holes when compared to other silicides, which leads us to expect a high drivability. PtSi on the Si mesa was used as the drain electrode, and PtSi on one side of the Si mesa bottom was used as the source electrode. A lightly doped p-type Si mesa with a resistivity of 30Ωcm was used as the channel in order to reduce the `off' current by virtue of its high resistivity in the sub-threshold region. The vertical channel was 55-nm-long and 10- or 30-nm-thick. The metal gate facing toward the Schottky source was 20-nm-thick Au/Cr. The gate oxide was 5- or 8-nm-thick SiO_2.

When operating in the `on' state, holes are injected from the source into the channel through the Schottky barrier and are transported in the accumulation layer under the gate oxide, which is induced by the gate-source voltage V_{GS}. The injected current consists of the tunneling current and the thermionic current. The

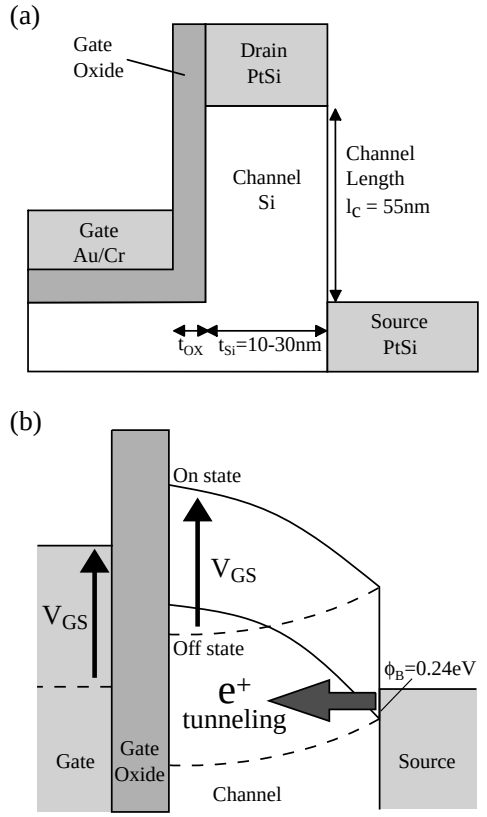

Fig. 1 (a) Cross-sectional structure of the vertical PtSi Schottky source/drain MOSFET and (b) band diagram in the `on' and `off' operating states.

probability of holes tunneling through the Schottky barrier is controlled by V_{GS}, which changes the Schottky barrier thickness due to the electric field, as shown in Fig. 1(b). V_{GS} also controls the thermionic current by lowering the Schottky barrier via the image force. In the `off' state, the Schottky barrier and the difference in the work function between the source and the gate electrodes blocks the thermionic emission of holes into the channel. In order to block the holes sufficiently, the work function of the gate must be lower than that of the source. Even in this situation, a small number of holes leak due to thermionic emission, and are transported along the opposite side of the Si mesa to the gate oxide.

3. Analytical Results

We approximated a one-dimensional device structure and calculated the drain current in the `on' state. In order to treat the electric field concentration at the source Schottky junction, we calculated a source Schottky junction depth up to which the electric field by V_{GS} is strong enough to generate the tunneling current. The

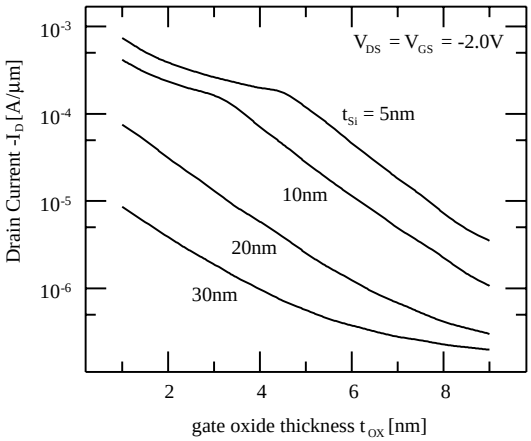

Fig. 2 Calculated device current for various thicknesses of the Si channel as a function of the thickness of the gate oxide t_{OX}. At this bias, the device current is in the saturation, and results are shown for the channel length of 50nm.

tunneling current becomes non-negligible at the electric field over 10^6V/cm, and the depth for this value is almost constant for structures and bias conditions (~5nm), calculated by the two-dimensional Poisson's equation. A method including a simple combination of the tunneling current at the source Schottky junction and the resistance of the accumulation layer in the Si channel is used here.

The drain current in the saturation region at various thicknesses of the Si channel is shown in Fig. 2. The drain current increases with decreasing the gate oxide thickness, which is originated from the exponential dependence of the tunneling current on the electric field at the source junction. Kinks in the lines for t_{Si} = 5nm and 10nm occur due to the resistance in the accumulation layer, because the slope of I_D is determined by the carrier injection from the source silicide at I_D < 150μA/μm, or the resistance in the accumulation layer at I_D > 150μA/μm. A shorter channel length can bring kinks to the larger drain current because of lower resistance in the accumulation layer. In such case, the resistance in the accumulation layer determined the drain current. This situation is the same as the conventional MOSFETs. Therefore, when a channel length becomes < 20nm, which requires t_{Si} < 5nm in order to suppress short channel effects, they will have the same drivability.

4. Fabrication Process

The fabrication process is as follows. The Si mesa pattern was formed by electron-beam lithography with PMMA resist. The metal mask for the mesa pattern was

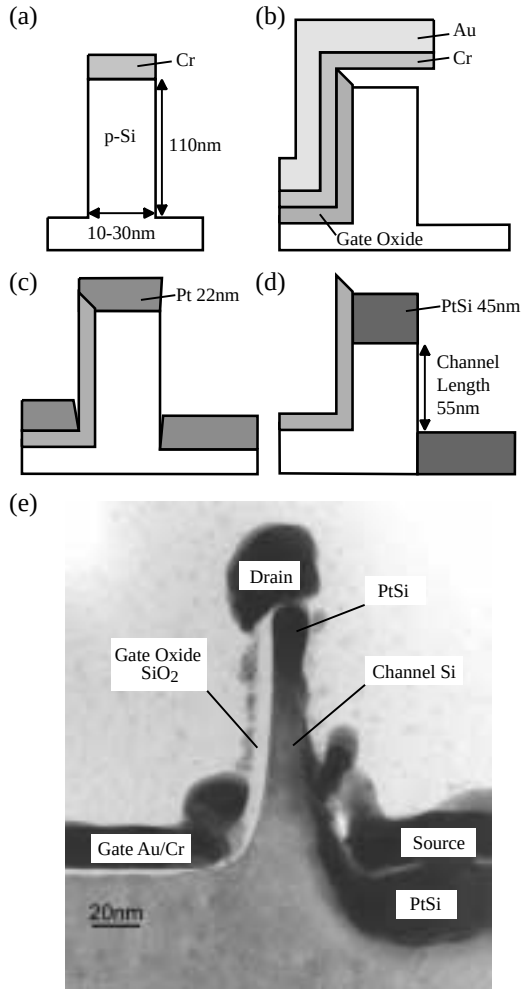

Fig. 3 (a), (b), (c) and (d) Process flow of the fabrication. (e) Cross-sectional TEM image of the fabricated device with 8-nm-thick gate oxide and 30-nm-thick Si channel.

formed with Cr by a lift-off process. The width of the metal line pattern was determined such that we could fabricate a 10- or 30-nm-thick Si mesa, taking into consideration the SiO_2 diffusion to the Si mesa during the fabrication of the gate oxide. Using this mask, a 110-nm-high vertical mesa was formed by CF_4 reactive ion etching, as shown in Fig. 3(a). After removing the metal mask using cerium ammonium nitrate, the substrate was cleaned using HPM ($HCl:H_2O_2:H_2O$=1:1:5) at 75°C for 10 minutes to remove any contamination and to form the native oxide on the mesa surface. A 5- or 8-nm-thick gate oxide was grown by thermal oxidation at 800°C after removing the native oxide using buffered HF. The gate-side SiO_2 surface was masked by tilt-deposited Au/Cr. In this deposition, Au/Cr did not cover the SiO2 at the source- and drain-side surfaces, because these surfaces were in the shadow of the Si mesa. Next the uncovered SiO_2 layer was removed by using buffered HF, as shown in Fig. 3(b). After removing the Au/Cr mask, a 22-nm-thick layer of Pt was deposited as the source/drain metal by electron-beam evaporation, as shown in Fig. 3(c), and this was then silicided for 10 minutes at 400°C in an N_2 ambient by rapid thermal annealing. The thickness of the PtSi was estimated at 45nm, which was twice that of the deposited Pt, and a 55-nm-long vertical channel was obtained using this process (i.e., the mesa height of 110nm minus the PtSi thickness of 45nm), as shown in Fig. 3(d). The unreacted Pt on the gate oxide was selectively etched using hot aqua regia. Finally, the gate and external source/drain electrodes were formed by depositing a 20-nm-thick layer of Au/Cr. The gate width was 1μm.

Figure 3(e) shows a cross-sectional TEM image of the fabricated device with the 8-nm-thick gate oxide and 30-nm-thick Si channel. The dark regions on the source and drain PtSi are the external source and drain electrodes fabricated together with the gate Au/Cr electrode. The TEM image shows that a vertical MOSFET with a channel length of about 55nm was obtained.

5. Measured Characteristics

Figure 4 shows the drain current curves for various gate-source voltages at room temperature for the devices. At V_{DS}=-1.5V and V_{GS}=-2.0V, the drain current and the transconductance of the 5-nm-thick gate oxide device are 30μA/μm and 40mS/mm, respectively. The above values for the 5-nm-thick gate oxide device are twenty times larger than those for the 8-nm-thick gate oxide device. The 5-nm-thick gate oxide device also has a lower value of V_{DS} at which the drain current starts to saturate. In the present device structure, in which the gate faces toward the source through the Si mesa and through the gate oxide, the gate oxide thickness is an essential device parameter because of the following criteria. (i) The thinner gate oxide increases the `on' current exponentially because the tunneling current is sensitive to the electric field at the source Schottky junction and the majority of the `on' current is the tunneling current in the fabricated devices. (ii) The saturation of the drain current starts at a lower value of V_{DS} due to the lower resistance in the accumulation layer induced by the thinner gate oxide.

The measurements were compared with the theoretical results of the dependence of the drain current

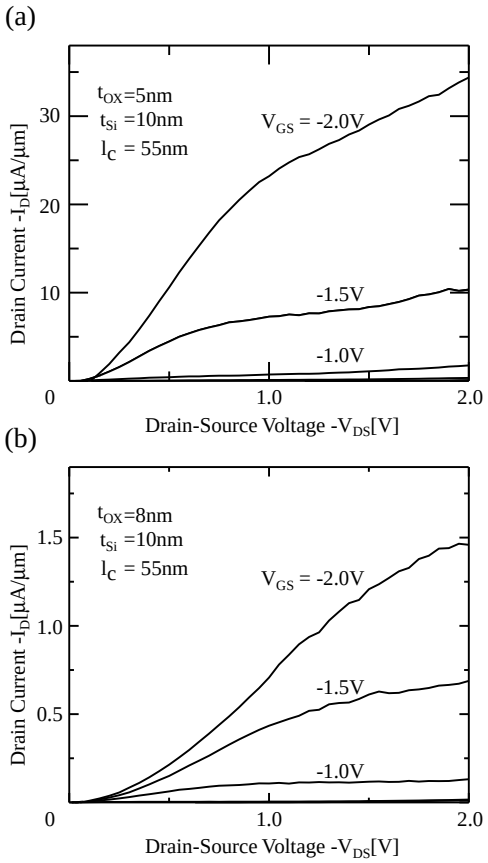

Fig. 4 Common-source drain curves of the PtSi vertical Schottky source/drain MOSFETs with (a) 5- and (b) 8-nm-thick gate oxide for various gate-source voltages. The vertical Si channel is 10-nm-thick and 55-nm-long.

on the gate oxide thickness for 10-nm-thick and 55-nm-long Si channel, as shown in Fig. 5. The measured and calculated dependencies on the gate oxide thickness show good agreement. The increase of the drain current as a function of the gate oxide thickness is 2.7times/nm in our measurements, which is the same as the value derived by calculation. Based on this comparison, further reduction in the gate oxide can increase the drivability. A drain current of over 150μA/μm can be obtained with a 3-nm-thick gate oxide.

6. Conclusion

P-type vertical PtSi Schottky source/drain MOSFETs with 5- or 8-nm-thick gate oxide were fabricated to evaluate the effect of the gate oxide thickness on the device characteristics. The device consisted of a 10-nm-thick and 55-nm-long Si channel, in which the

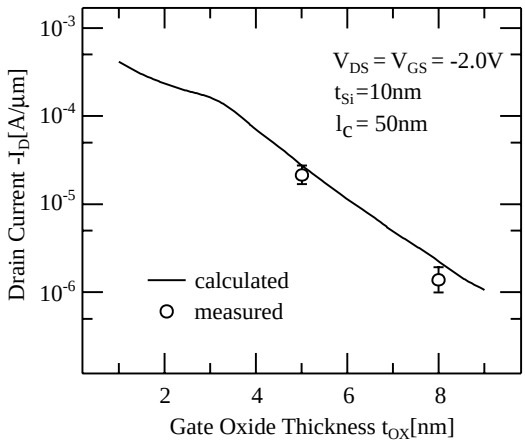

Fig. 5 Measured and calculated drain current curve as a function of the gate oxide thickness at V_{DS}=$V_{GS=}$-2.0V, when the drain current is in saturation.

metal gate faced toward the Schottky source. The dependence of the drain current on the gate oxide thickness was compared between the measurements and calculation, and they showed good agreement. Based on this comparison, an improvement in the device characteristics can be achieved by using a thinner gate oxide, and a drivability of about 150μA/μm will be obtained with a 3-nm-thick gate oxide.

Acknowledgments

The authors thank Emeritus Professor Y. Suematsu of the Tokyo Institute of Technology for encouragement during this work. We also thank Professors K. Furuya and S. Arai, and Associate Professors Y. Miyamoto and M. Watanabe for fruitful discussion. One of the authors (MT) was supported by JSPS Research Fellowships for Young Scientists.

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