QNERC NEWSLETTER

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TOKYO INSTITUTE OF TECHNOLOGY

QNERC Quantum Nanoelectronics Research Center

Focus on 2D materials

A chance meeting at a nanotechnology conference in Switzerland in 2008 between QNERC's Professor Shunri Oda and Professor Kaustav Banerjee, director of the Nanoelectronics Research Lab at UC Santa Barbara, has led to a fruitful collaboration between them. Now, Banerjee is making his second visit to QNERC funded by an Invitation Fellowship of the Japan Society for the Promotion of Science.

"The fellowship evolved out of working on several projects with QNERC," says Banerjee. "I'll be exploring with Professor Oda what we might combine of his research into low-dimensional materials, particularly 0-D quantum dots and 1-D quantum wires, with my work into 2-D crystals."

Two-dimensional (2D) crystals are atomically thin materials, the most well known being graphene—an atomically thin layer of carbon discovered by scientists at the University of Manchester who were awarded the 2010 Noble Prize in Physics.

"2D materials exhibit a wide range of properties, including semiconductor and superconductor characteristics," says Banerjee. "And because they are atomically thin, and come with a range of band gaps, somewhere between one and two electron volts, you can do a lot of interesting things with them in electronics."

Kaustav Banerjee

His research group in Santa Barbara synthesize 2D materials and conduct ab initio modeling to design and fabrication devices and circuits.

In addition to being transparent, flexible and stable at ambient temperatures, these so-called layered materials can be isolated relatively easily from their bulk constituents, similarly to mechanical exfoliation of graphene from graphite.

"We want to marry 2D and 1D materials and build some hybrid structures," says Banerjee. "This could lead to some interesting devices in both the electronics and optoelectronics areas."

The ultimate aim is to replace silicon with 2D materials for the next generation of transistors with sub- 8nm channel lengths.

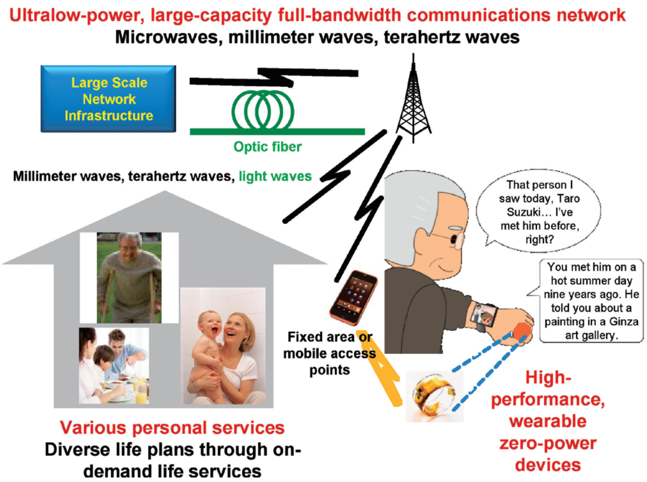
Towards an Ageless Society

Japan's Ministry of Education, Culture, Sports, Science & Technology (MEXT) has initiated a joint academia-industry 10 year research project to advance the welfare and happiness of the people living in Japan.

MEXT selected 12 proposals for Centers of Innovation (COI) and a further 14 as COI Trialists from which some will be picked this year as additional members of the project. Professor Shunri Oda is the research leader of one such trialist group with the goal of fostering a "smart society" where citizens of all ages are provided with the means to be productive and enjoy life until the end of their days, thus creating an "ageless society."

If the group is selected for COI, the Oda will have the responsibility of gathering scores of experts from Tokyo Tech and other prestigious academic institutes from fields as diverse as electronics, physics, information processing, and management technology. He will work jointly with Shigeyuki Akiba of KDDI R&D Laboratories, who is forming a similar group of researchers from industry, and which includes such corporate names as NTT and NEC.

The emphasis of the project is to develop information communications technology in the microwave, millimeter and terahertz wave bands to deliver a variety of new on-demand services customized for individuals.



This success of the project will necessitate the development of highly distributed stream- processing of Big Data, any-place, any-time communications in all frequency bands, and zero-power wearable devices that require no charging, relying instead on low-power devices utilizing energy harvesting.

"In choosing our goal for such a long-term project, we decided it had to be something not easily achievable, something that the questions it raises have no obvious answers," says Oda. "So by definition it is a high-risk project, but with academia and industry working in unison. We believe it is achievable."

Akira Matsuzawa

Director, QNERC;
Professor, Tokyo Tech

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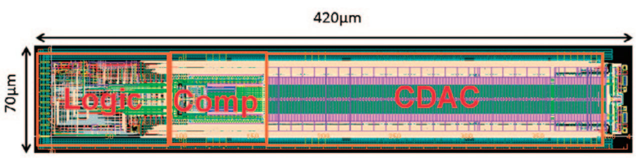
Frequency, performance, and power scalable CMOS 12 bit SAR ADC

Akira Matsuzawa and his colleagues have developed the frequency, performance and power scalable CMOS 12 bit SAR ADC with world's top FoM and occupied area.

ADC is the most important analog IP for almost all electric systems. Conventionally ADC is designed dedicated to the required performance, such as frequency and SNR and results in increase of development costs. Therefore a frequency, performance, and power scalable ADC based on 12 bit SAR ADC was developed to address this issue [1].

The resulting 12 bit ADC in 65nm CMOS occupies a small area of 0.03mm^2 and has a low power dissipations of 2.2/4.6 mW at high conversion rates of 50/70 MS/s. It also achieves the world's smallest DC FoMs of 28/33 fJ/conv with 0.8/1.0 V supply.

Therefore, the SAR ADC developed in this research will increase the design efficiency for the future mixed signal LSI circuits.



12bit SAR ADC using 65nm CMOS

[1] S. Lee[1], H. Kawaraguchi[1], T. Hirato, M. Miyahara[1], and A. Matsuzawa[1,2], "A 12b 50/70 MS/s 2.2/4.6 mW 0.03mm^2 CMOS SAR ADC for a frequency, performance, and power scalable ADC," Solid State Devices and Materials,H-2-2, Fukuoka, Japan, Sep. 2013.

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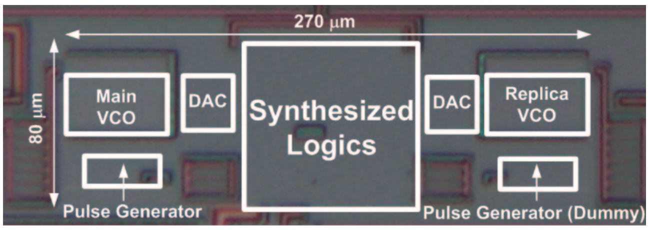
Sub-picosecond CMOS low power time-to-digital converter and sub-picosecond jitter, small area and low power CMOS timing generator

Small power and area, fine resolution, and low jitter timing measurement and timing generator circuits are very important core elements for many electrical systems such as particle detectors, radar systems, 3D recognition, frequency synthesizers, and clock generators for LSI circuits.

Akira Matsuzawa and his colleagues have developed a sub-picosecond CMOS time-to-digital converter (TDC) that converts a time interval into the charge of a sampling capacitor of a SAR ADC by using a charge pump [1]. The chip was fabricated in 65nm CMOS and achieved 0.84 ps LSB with a low power consumption of only 2.47 mW and a small core area of 0.06 mm^2. The DNL is -0.7/1.0 LSB with 8-bit range.

Also, the sub-picosecond jitter and small area and power CMOS timing generator using injection locking method was developed [2]. The chip was fabricated in 65 nm CMOS and achieved low jitter of 1.8 ps with small power of 1 mW and small area of 0.02 mm^2. The circuit can be composed with automatic ray out synthesis and suitable for future IP core applications.



Chip micro-photograph

[1] Zule Xu[1], SeungJong Lee[1], Masaya Miyahara[1], and Akira Matsuzawa[1,2], "A 0.84ps-LSB 2.47mW Time-to-Digital Converter Using a Charge Pump and a SAR-ADC," IEEE Custom Integrated Circuits Conference, 23-2, San Jose, Sep. 2013.
[2] W. Deng[1], A. Musa[1], T. Siriburanon[1], M. Miyahara[1], K. Okada[1], and A. Matsuzawa[1,2], "A 0.022 mm^2 970 µW Dual-Loop Injection-Locked PLL with -243 dB FOM Using Synthesizable All-Digital PVT Calibration Circuits," IEEE International Solid-State Circuits Conference (ISSCC), pp.248-249, San Francisco, CA, Feb. 2013.

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Shigehisa Arai

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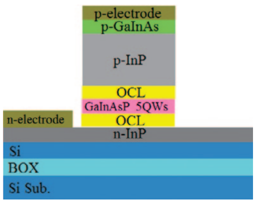
GaInAsP/Si Hybrid Laser by Plasma Activated Bonding

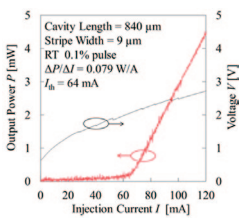
The integration of III-V active devices on a Si platform utilizing direct bonding is an attractive way to realize large-scale photonic integrated circuits. Because plasma activated bonding (PAB) is expected to have a higher bonding strength at a lower heating temperature as compared to conventional bonding methods, PAB is attractive for the reduction of non-radiative recombination centers in the III-V active region caused by thermal expansion during the bonding process.

Shigehisa Arai and his colleagues have been engaged in low-temperature PAB process of GaInAsP multiple-quantum-well structure on a SOI wafer to realize GaInAsP/Si hybrid laser. By reducing the process temperature to 150°C, thermal damage was fairly reduced while the bonding strength of larger than 0.5 MPa was obtained. A threshold current density of 850 A/cm^2 (170 A/cm^2 per quantum-well) and the differential quantum efficiency of 10%/facet were obtained.

These results show that the low-temperature plasma activated bonding (PAB) is very promising for building-up a photonic platform consisting of functional photonic devices such as semiconductor optical amplifiers and functional passive optical elements.



Schematic and cross-sectional structures of GaInAsP/Si hybrid laser by Plasma Activated Bonding (PAB).



Lasing properties of GaInAsP/Si hybrid laser by Plasma Activated Bonding (PAB).

Yusuke Hayashi[1], Ryo Osabe[1], Keita Fukuda[1], Yuki Atsumi[1], JoonHyun Kang[1], Nobuhiko Nishiyama[1], and Shigehisa Arai[1,2]

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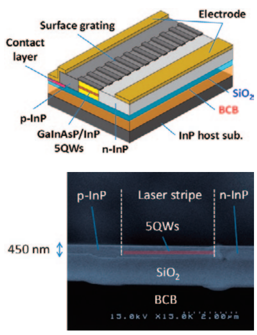
Jpn. J. Appl. Phys., vol. 52, no. 6, pp. 060202-1-3 (2013).

Lateral-Current-Injection Type Laser and Photodiodes for Optical Interconnection

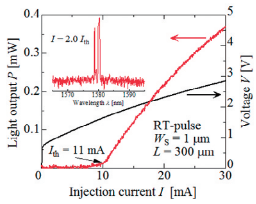
Ultra low-power consumption light sources and low-noise photodetectors are essential to exploit the advantages of optical systems in short-reach and on-chip optical interconnections. In particular, high-index contrast, strong optical confinement structures—composed of a thin semiconductor core (membrane) and polymer claddings—are of interest to achieve low threshold operation of semiconductor lasers.

Shigehisa Arai and his colleagues are conducting research on electrically driven membrane lasers for on-chip optical interconnection. They successfully realized room-temperature pulsed operation of GaInAsP/InP lateral current injection (LCI) type membrane DFB lasers with surface gratings. A threshold current of 11 mA was attained for a device with five quantum-wells, stripe width of 1 μm, and a cavity length of 300 μm. The room-temperature continuous-wave operation of LCI membrane Fabry-Perot cavity laser was also achieved with a relatively low threshold current of 3.5 mA (threshold current density of 500 A/cm^2, 100 A/cm^2 per quantum-well) and a differential quantum efficiency of 11% per facet.

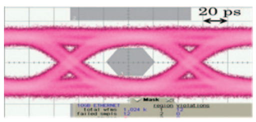


Schematic diagram (left) and cross sectional SEM view (right) of LCI membrane DFB laser structure.

Photodiodes with a lateral junction structure were also realized with responsivity of 0.27 A/W at 1550 nm. A 3-dB bandwidth of 8.8 GHz and a clear eye opening at 10 Gb/s at Vbias = -2 V were obtained.



Lasing properties of lateral-current-injection (LCI) membrane DFB laser.



Eye diagram at 10 Gb/s (V_{bias} = -2 V) of a lateral junction photodiode.

These experimental results suggest that this membrane structure has great potential for photonic global wiring in future LSI circuits.

Takahiko Shindo[2], Mitsuaki Futami[2], Tadashi Okumura[2], Ryo Osabe[2], Takayuki Koguchi[2], Kyohei Doi[2], Tomohiro Amemiya[1], Nobuhiko Nishiyama[2], and Shigehisa Arai[1,2]

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IEEE Photon. Technol. Lett., vol. 25, no. 13, pp. 1282-1285 (2013).
Jpn. J. Appl. Phys., vol. 52, no. 11, pp. 118002-1-3 (2013).

Yukio Kawano

Associate Professor, Tokyo Tech

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Nanoscale Terahertz and Infrared Imaging beyond the Diffraction Limit

Potential applications of terahertz (THz) and infrared (IR) imaging include remote safety inspection, medical care, and nondestructive analysis of materials and bio-molecules. However, the fundamental issue of low imaging resolution must be resolved for examination of nano-materials and biological cells, and molecules.

Yukio Kawano and his colleagues at QNERC, Tokyo Tech have developed near-field THz and IR imaging systems (Fig. 1), with spatial resolution 20–400 nm, which is far beyond the diffraction limit. The system was used to visualize and analyze semiconductors, metal antennas, and polymers. The THz and IR near-field images were in good agreement with simulation results, demonstrating the potential applications of THz and IR imaging for exploring carrier transport, antenna properties, and higher-order structures of polymers.

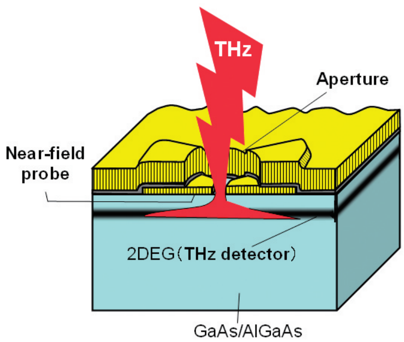

Fig. 1.
Schematic view of the integrated near-field THz imager

Combining with simultaneous THz/IR spectroscopy makes this imaging technology even more powerful. Kawano plans to incorporate aspects of his previous research on wide-band frequency-tunable graphene detectors (Fig. 2).

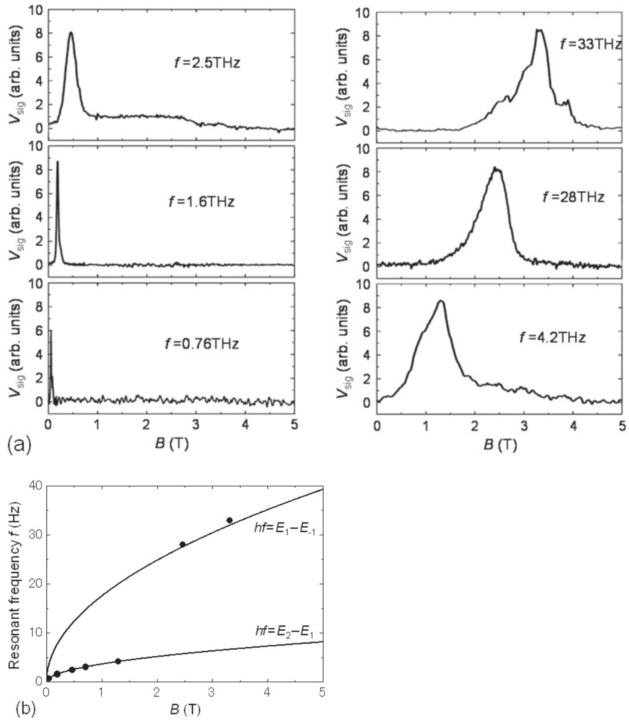

Fig. 2.
(a) THz and IR detected signal V_{sig} as a function of magnetic field *B* at f=0.76, 1.6, 2.5, 4.2, 28, and 33THz for the graphene device.
(b) Resonant frequency *f* versus magnetic field *B* for the inter-level transitions in the graphene. $hf=E_2-E_1$, E_1-E_{-1}. The theoretical (curves) and experimental (black circles) results were plotted.

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Terahertz Waves: A tool for Condensed Matter, the Life Sciences and Astronomy
Contemporary Physics, 54, 143-165, (2013).
Digital Object Identifier (DOI): 10.1080/00107514.2013.817194

D. Suzuki[2], **S. Oda**[1] **and Y. Kawano**[1]

GaAs/AlGaAs field-effect transistor for tunable terahertz detection and spectroscopy with built-in signal modulation
Applied Physics Letters, 102, 122102-1-4, (2013).
Digital Object Identifier (DOI): 10.1063/1.4798329

Y. Kawano[1]

Wide-Band Frequency-Tunable Terahertz and Infrared Detection with Graphene
Nanotechnology, 24, 214004-1-6, (2013).
Digital Object Identifier (DOI): 10.1088/0957-4484/24/21/214004

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Diameter modulation of germanium nanowires by temperature variation

Germanium nanowires have a unique advantage over other semiconductor nanowires: high hole mobility and relatively low growth temperature, which are attractive properties for device fabrication on low melting point flexible substrates. Shunri Oda and co-workers at QNERC, Tokyo Tech synthesized germanium nanowires via a two-step growth technique, whereby growth was initiated at 300 °C and subsequently lowered to 260 °C. Using this technique, they showed that nanowire diameters can be modulated by growth temperature and investigated the crystallinity difference between tapered and straight structure in a single nanowire. They also developed a model to elucidate how the nanowire diameter decreases as the growth temperature decreases.

Fig. 1 shows an image of a germanium nanowire grown via the two-step growth technique. The nanowire base diameter is large at first and becomes narrower towards the nanowire tip as the growth temperature decreases. Fig. 2 illustrates a model of nanowire diameter modulation via the two-step growth technique.

Modulated nanowire diameters will be useful for simultaneously observing the band gap changes from "indirect" to "direct" in a single nanowire.

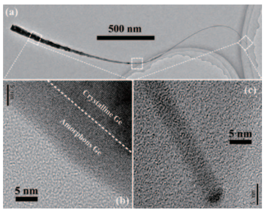

Fig. 1

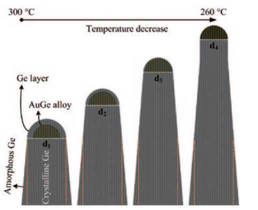

Fig. 2

Figure captions:

Fig. 1. Germanium nanowire grown via the two-step growth technique. For the indicated regions from left to right, the nanowire diameters were measured to be 38, 14, and 4 nm, respectively. (b) Magnified image of the tapered region near the nanowire base, confirming that this region contains crystalline and amorphous germanium. (c) Magnified image of the straight region near the nanowire tip, confirming that this region contains only crystalline germanium.

Fig. 2. Model showing the mechanism of nanowire diameter modulation via the two-step growth technique. At higher temperature, nanowire diameter is determined by the size of AuGe alloy coated with germanium layer. As the growth temperature decreases, germanium layer becomes thinner and finally disappear and the nanowire diameter decreases gradually ($d_1 > d_2 > d_3 > d_4$).

Marolop Simanullang, Koichi Usami, Tetsuo Kodera, Yukio Kawano, and Shunri Oda

Microscopic study of germanium nanowires grown via gold-catalyzed chemical vapor deposition below the eutectic temperature
Journal of Crystal Growth 384, 77 (2013).
Digital Object Identifier (DOI): 10.1016/j.jcrysgro.2013.09.009
Quantum Nanoelectronics Research Center, Tokyo Institute of Technology,

Dual Function of Si Quantum Dots for Integrated Qubits

Recently, quantum bits (qubits) with using electron spins in semiconducting nanostructures are being studied by many researchers because of their scalability and long coherence time for quantum computing. Many quantum dots (QDs) are integrated to be used for not only qubits but also sensors to identify the position of the electron. In addition to such QDs, many gate electrodes should be integrated to the qubit device to control the electrochemical potential of each QD and tunnel barriers between the QDs. These large numbers of gate electrodes and QDs for qubits and sensors occupy a large space in the device, which would be a problem in its integration to achieve a quantum information processor. Therefore, the technological development of QDs by multifunctionalization is required to reduce the number of gates and integrate many QDs.

Shunri Oda and co-workers at Tokyo Tech in collaboration with Arakawa laboratory in Tokyo University have demonstrated gating and charge sensing functions of a lithographically defined Si QD.

Figure 1 shows (a) a schematic diagram, (b) scanning electron microscope image of the device, and Coulomb peaks in I_{DQD} - $V_{gl,gr}$ traces, and (c) the gating function of an integrated single QD (SQD) to double QD (DQD). Figure 2 shows (a) a stability diagram of the DQD and (b) the differential conductance of the SQD. The SQD detects the single-electron transitions in the DQD with its charge sensing function.

This result provides an important step for future integration of qubits in semiconductor.

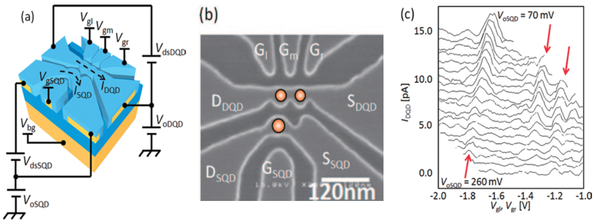

Fig. 1.

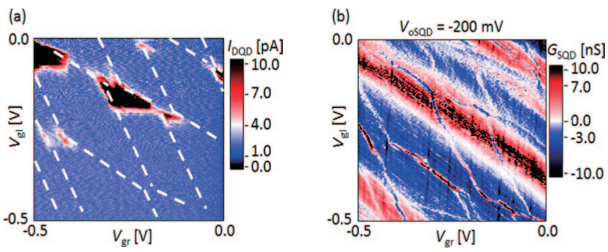

Fig. 2.

Tomohiro Kambara[1], Tetsuo Kodera[1, 2, 3], Yasuhiko Arakawa[2,4], and Shunri Oda[1]

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Dual Function of Single Electron Transistor Coupled with Double Quantum Dot: Gating and Charge Sensing
Japanese Journal of Applied Physics **52**, 04CJ01 (2013).
Digital Object Identifier (DOI): 10.7567/JJAP.52.04CJ01

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