Single Electron Devices Based on Nanocrystalline Silicon

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Abstract nano-crystalline Si dots of dimensions of 8nm have been incorporated into a variety of Coulomb blockade and floating gate memory devices. Structures include vertical transistor, planar electrode, nanoscale channel junction and 2-gate trench structure. Ballistic transport, Coulomb oscillation and memory effects are clearly demonstrated

I. Introduction

As the ultimate goal in scaling of microelectronics, single electron devices have the possibility to drastically improve memory and logic device performance by high device density, low power consumption and improved integration. With current scaling trends in MOSFET production there is the inevitable need to understand and optimize devices which operate with only a statistically small number of electrons. Particularly complex factors such as Coulomb blockade, quantized energy levels, defect states, and background charge must be understood as well as optimal device structures designed. Si based nanoscale devices are strong contenders due to existing Si process infrastructure as well as the nearly perfect interface between SiO_2 insulator and Si. The latter advantage is paramount to success since single electronic devices are obviously sensitive to local and background charged defects. Several groups have demonstrated single electron effects in Si systems. Examples include charge stored in nanoscale Si dots above FET channel [1,2], memory devices based on charge through complex percolation paths of several nm thick SOI [3], and e-beam lithography defined SOI junctions (30nm scale) [4]. However there is a great need for such devices to demonstrate cost-effective processing with high reproducibility, which is typically strongly dependent on feature size. At nano-scales, the control of dimensions by lithography is difficult and hampered by slow throughput. Thus a self limiting gas phase nano-crystalline Si (nc-Si) growth is attractive. Plasma enhanced CVD with pulsed gas source readily deposit 8+1nm nc-Si over a large area [5]. The advantage of this process over other CVD processes is a lower nc-Si size dispersion as well as not co-depositing a-Si, which acts as charged defect sites. Since the exact location of deposited nc-Si is not controlled, it is necessary to study various approaches in device design which best utilize such nc-Si. Four devices will be discussed which study electron transport through nc-Si or its use as a memory node. The first is a vertical structure in which current is passed through nc-Si isolated in a hole in a gate electrode. The next deposits nc-Si dots between Silicon-on-Insulator (SOI) electrodes with 15-30nm gap. The third uses nc-Si as a floating gate above an SOI channel with SET tunnel barrier constriction. The fourth approach uses a 2-gate trench structure to localize active area, control overall current level and allows high source-drain bias, which is important for device applications.

II. Results and Discussion

IIa. Vertical SET structure

Since control of film thickness is much finer than lateral resolution of lithography, vertical structures can allow precise control of tunnel barrier thickness, which is a critical parameter for current level reproducibility. Nc-Si is simply incorporated into vertical structures by deposition into e-beam lithographically defined holes in gate electrode. Dots that are not deposited into holes are not electrically active. The synthesis starts with heavily doped (0.002 Ωcm) Si(100) with 25nm of thermal oxide. Onto this 20nm of P-doped ($10^{18}/cm^3$) a-Si is deposited for gate electrode. To eliminate charged defect states, a-Si is crystallized into large 100-200nm long grains by solid phase crystallization (SPC) method of annealing at 700ºC (4hrs) then 900ºC(1hr). 30 nm of SiO_2 from PECVD of tetraethoxysilane is then deposited. A hole is then defined by e-beam lithography (60x60nm) of positive resist ZEP520. Within the pattern the top oxide is etched by ECR-RIE with CF_4 , then poly-Si gate electrode

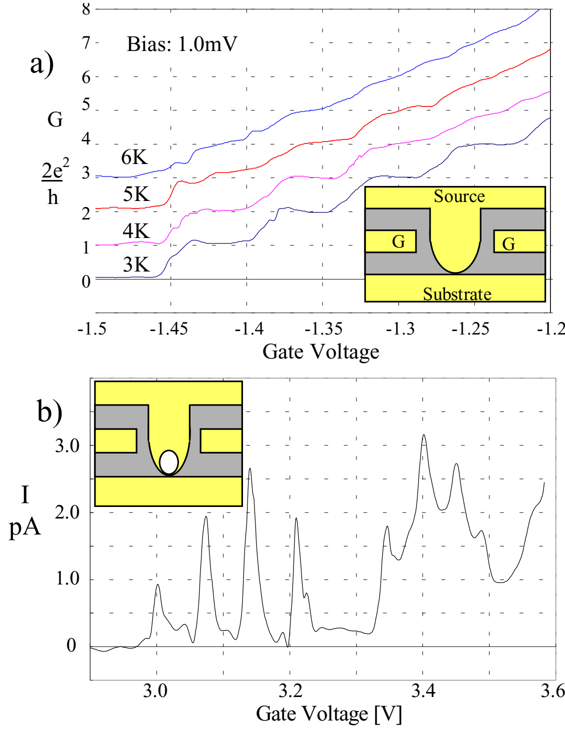


Figure 1. a) Conductance quantized steps for vertical transisor without nc-Si. b) Gate oscillations for current passing through nc-Si with native oxide tunnel barriers indicating Coulomb blockade effects.

is selectively etched by direct reactive plasma etch (CF_4+10%O_2) followed again by ECR-RIE (CF_4) etch of lower thermal oxide. Fluoride defects are removed by 20min 800C oxidation, stripped by 1%HF, followed by another 20nm oxide deposition. This oxide is again etched by ECR-RIE (CF_4). In the case of this small structure, the last etching is not vertical but tapered, allowing the bottom substrate contact to be 10nmx10nm, which is confirmed by cross-sectional SEM. Into this hole nc-Si is deposited by RECVD as well as a-Si, which is subsequently crystallized by SPC method. Evaporated aluminum is used for contacts.

Remarkable results are seen with the structure depicted in Figure 1a)., in which nc-Si is not deposited. In this case, clear ballistic transport steps in conductance G is quantized to $G=N\times 2e^2/h$, where N is the integer. Figure 1 shows the current as a function of V_g at V_b=1 mV, for various values of temperature: 3K, 4K, 5K, and 6K. For clarity, traces are shifted vertically by $2e^2/h$. For ballistic transport the channel width and length must be narrower than the inelastic mean free path. The carrier concentration N is ~10^{17} /cm^2 and the carrier mobility μ is ~10^3 cm^2/V·s at 5 K. From these values, the Fermi energy is 63 meV, Fermi length is 11 nm, inelastic mean free path $l_{in} = \mu\hbar\sqrt{2\pi N}/e$ =~300 nm , and elastic mean free path $l_{el} = G_s h/2e^2\sqrt{\pi N}$ =~45nm, where G_s is the sheet conductance, $\hbar$ is the Dirac constant, and h is the Planck constant. These results demonstrate that Si is readily synthesized to the small scale and low defect level that allows transport without scattering. This has significant applications for high speed devices using Si.

For the structure that incorporates nc-Si, which is surrounded by native oxide tunnel barriers, Coulomb blockade effects are seen. In current-voltage measurement a ±1V blockade is readily observed which is much larger than can be expected from a simple Coulomb blockade. The large blockade region is likely a result of the nc-Si being undoped and carriers having to overcome the bandgap. At bias high enough to overcome bandgap barrier, oscillation peaks and steps with a period of approximately 700mV can be seen in Figure 1b). These oscillations are consistent with Coulomb blockade limiting transport through nc-Si dot.

IIb. Nc-Si between planar SOI electrodes

Although exact dot location cannot be controlled, dots in contact with each other will have the same tunnel barrier and potential drop, thus it is possible to incorporate nc-Si dots in a

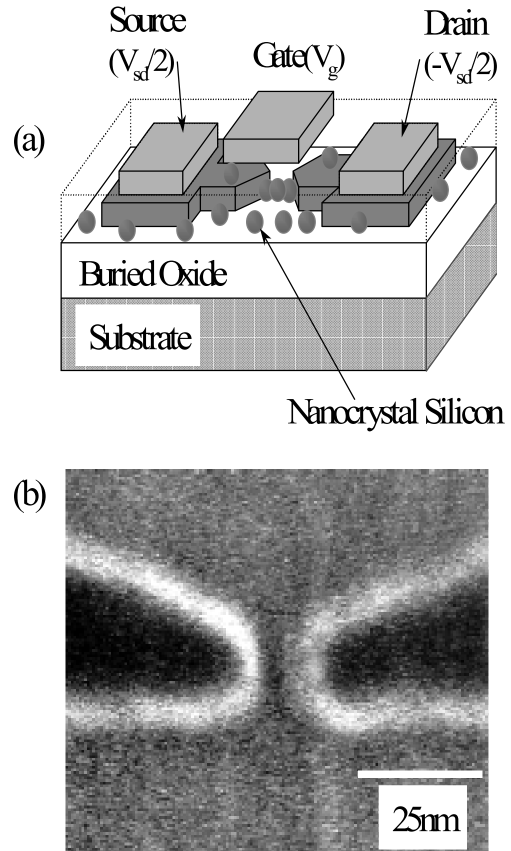


Figure 2. a) Schematic of device based on nc-Si dots being deposited between nano-scale electrodes. SEM picture of e-beam defined electrodes with 15nm gap.

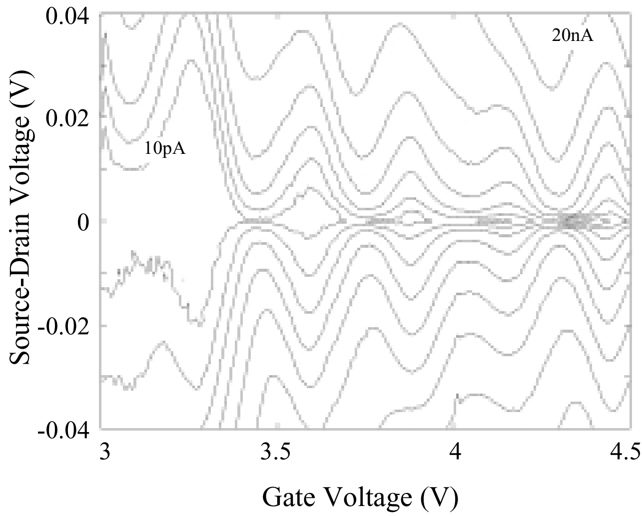


Figure 3. Logarithmic contour plot of source-drain current as a function of gate and source drain bias clearly showing Coulomb diamonds.

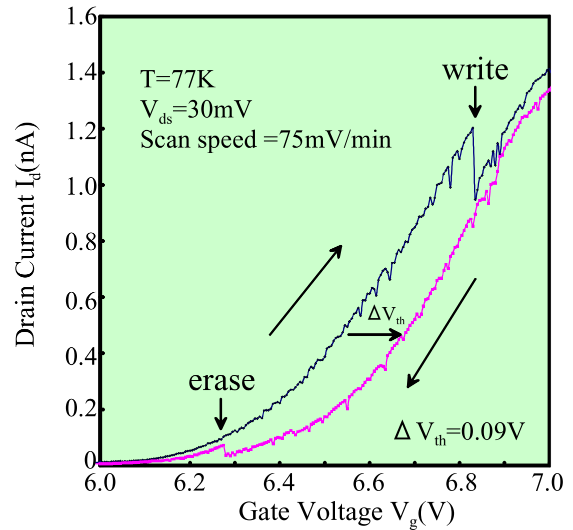
planar device. Overall scheme and SEM picture of electrode gap are shown in Fig.3. The synthesis begins with thinned (30nm) Silicon-on-Insulator substrate which is heavily doped ($3x10^{19}cm^{-3}$). Onto this electrodes with 30-15nm gaps are defined by direct writing of RD2000N resist followed by ECR-RIE etching with CF_4 gas. Fluoride defect states are removed by 800ºC oxidation. SiO_2 gate oxide of 50nm is deposited by PECVD. Aluminum is used for source, drain and gate contact. As in the previous vertical device, a large blockade due to the intrinsic bandgap of nc-Si dots is seen to be 1.3V, which is larger than Si bandgap. This increase in bandgap is consistent with quantum confinement energy for dots of 8nm diameter. Figure 3 shows contour plot of I_{sd} as a function of V_{sd} and V_{gate}. Clear Coulomb diamonds are observed with a period of about 310mV. The period is slightly reduced at higher diamond levels (more stored electrons) which would be expected for quantized energy levels. The change in energy of the dot (E_{gd})is given by

$$\Delta E_g = \frac{C_g}{\Sigma C} \Delta V_g \approx 0.186 \Delta V_g \qquad (1)$$

where C_g = 0.7aF is the gate capacitance, C_s and C_d = 1.5aF are the junction capacitance and C_{sub} = 0.07aF is the substrate capacitance. For 310mV period, •Egd≈58meV, which is consistent if both Coulomb charging energy and quantum energy levels are considered.

IIc. Nc-Si dot as floating gate memory

Another approach to single electron devices is to store charge in a floating gate above a narrow channel which can shield applied gate bias and



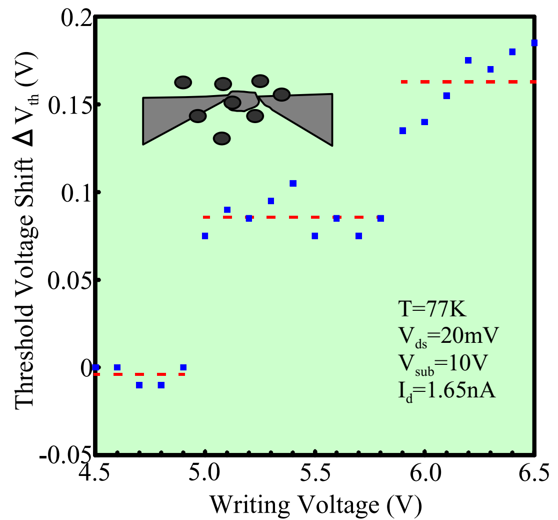


Figure 4. a) Onset of threshold voltage for narrow SOI channel junction with nc-Si dots acting as floating gate memory. Clear steps for writing are seen. b) Shift in threshold voltage as a function of writing voltage.

result in a shifted Threshold voltage (V_{th}). This has the distinct practical advantage of room temperature operation as well as voltage gain. To localize the memory node to be effected by only several nc-Si, a 30nm thick SOI channel is defined by e-beam lithography to form a 20x20nm Si island with two constriction/tunnel barriers. This forces an overall current minima to be spatially confined. This is schematically shown in the inset of Figure 4b). The device is synthesized as in Section IIb with the exception of self-aligned doping implantation allowing p/n junction for transistor operation. Gate oxide thickness is 50nm. Figure 4a). shows that a V_{th} shift of 90mV due to charge stored in nc-Si is observed. The step observed at 6.8V strongly suggests that the shift is due to a single electron. The retention time is at least 4 hours at 77K.

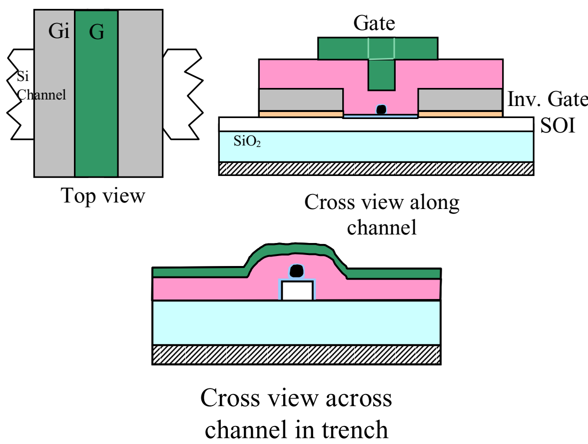


Figure 5. Schematic of 2-gate trench nc-Si floating gate memory device. Trench width is between 100-300nm, SOI channel thickness and width 30nm.

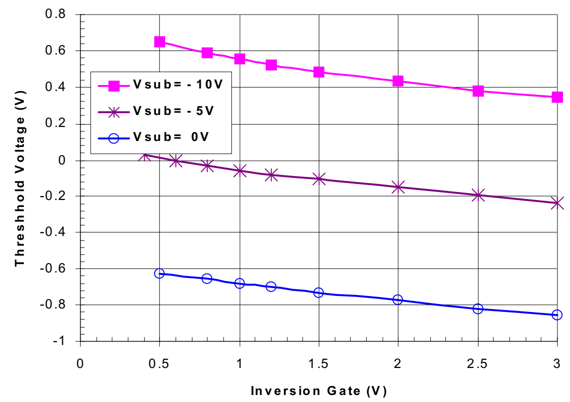


Figure 6. Threshold voltage as a function of Inversion Gate and Substrate bias for 200nm wide trench structure.

Figure 4b) shows shift in V_{th} as a function of gate bias with steps being seen at 1V increments which correspond to a Coulomb charging energy of 20meV. Deviation from steps are likely due to background charging of nc-Si in proximity of constriction. Such data shows that it is possible to use nc-Si dots in memory where only a few electrons are involved.

IId 2-gate trench device with nc-Si floating gate memory

A unique approach to optimizing single electron memory is the use of a two gate trench structure shown schematically in Figure 5. The benefits of a 2-gate approach are to confine active area to just several dots, allow high V_{sd} for device integration, independent control of carrier concentration outside of active region, and adjustment of V_{th}. To synthesize such a device, a narrow 30nm channel on 20nm thick SOI is defined by e-beam lithography and ECR-RIE etching. A thermal oxide and large poly-Si "inversion" gate is deposited. A 100-300nm wide trench is defined by e-beam lithography and etched into the inversion electrode over the channel. Nc-Si dots are deposited into the trench which is then covered by a CVD gate oxide and gate electrode.

The electric potential fields within such a device are complex without analytical solution, however can be readily modeled with the numerical solution of Poisson's and continuity equations. For such analysis a commercial 2 and 3 dimensional program Taurus 2.1 by TMA industries was utilized. Primarily discussed here are the modeled advantages of a 2gate trench design. For such a simulation important

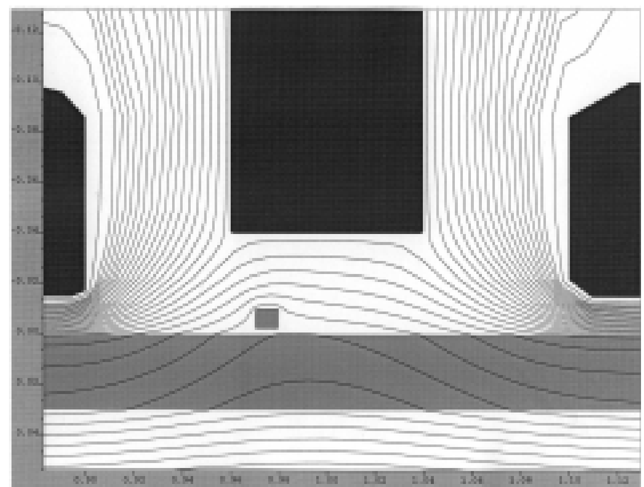


Figure 7. Calculated 2D potential profile in active region of 200nm trench showing shielding of charge in nc-Si. Vg=0V, Vgi=1.5V, Vsub=-5V.. Contours are at 50mV

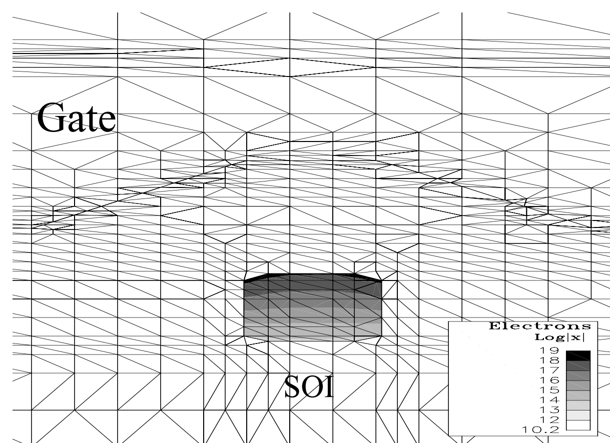


Figure 8. Calculated electron density of channel in cross-section (y-z plane, where x-axis is length of channel) under center of device gate electrode. Plane extracted from 3-D simulation to show carrier density on side of channel is negligible.

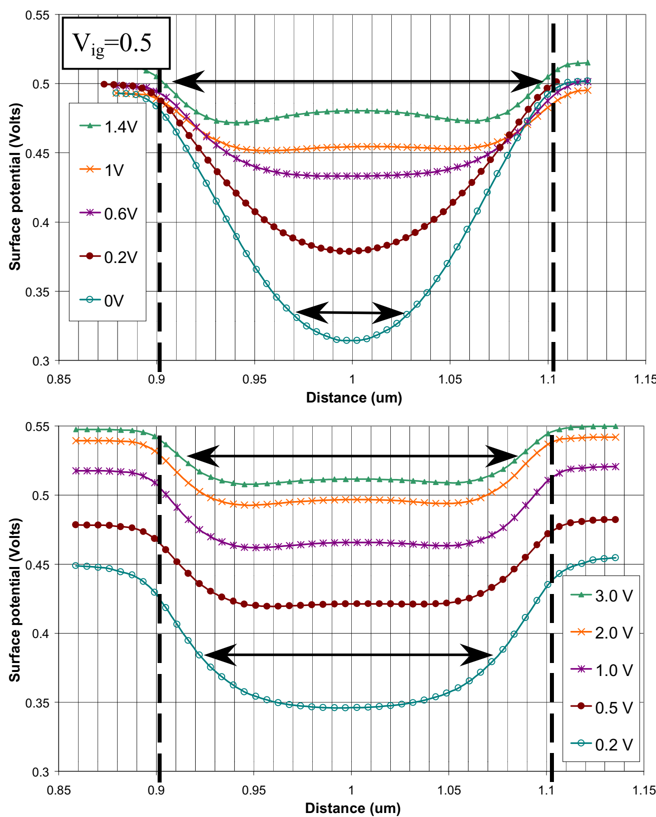


Figure 9. a) Calculated surface potential on SOI channel in active region of device as a function of lateral distance along channel. Lines with arrows show the length of active region. Shown voltage series is applied Gate voltage. Vinv=1.5V, Vsub=-5V. Dashed lines indicate boundaries of 200 nm wide trench b) Calculated surface potential when control and inversion gate are ramped together.

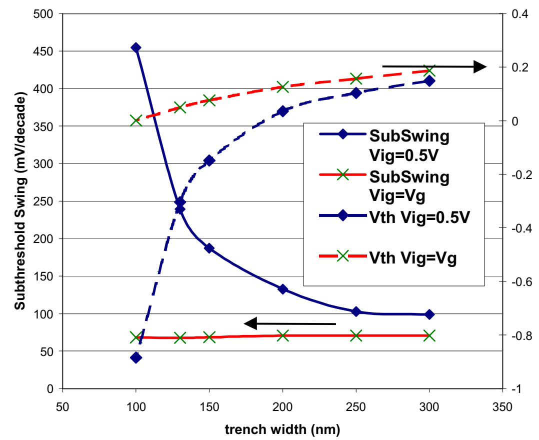


Figure 10. Calculated Vth (dashed lines) and subthreshold swing (solid lines) as a function of trench width. Severe short channel like effects are seen when inversion gate voltage is kept constant but are eliminated when control and inversion gate are ramped together.

dimensions are thickness inversion oxide 15nm, thickness gate oxide 40nm, buried oxide thickness 400nm, n^+ doping $1x10^{19}$, p^- doping $1x10^{16}$, Polysilicon gates. Simulation shows that V_{th} is equally shifted by Substrate or Inversion Gate bias (roughly 100mv Vth shift/Volt bias). However, adjusting V_{th} by negative substrate bias has the advantage of keeping carriers on top of the channel where shielding from nc-Si is effective and allows tuning of overall carrier level with inversion gate. However, the use of substrate bias has the difficulty of being unable to incorporate into complementary metal-oxide semiconductor (CMOS) design. The low power consumption would have to rely on low current levels and long memory retention times.

Figure 7 shows a representative 2D solution of the 2 gate structure potential profile showing shielding from the nc-Si dot. Figure 8 shows the electron density profile of a cross section of the channel under the gate from 3-D simulation. This geometry corresponds to the third scheme of Figure 5. Particularly important is the fact that carriers are not generated on the side wall of the channel where they would not be shielded by nc-si dots. With control gate oxide thickness thinner than the height of the channel side wall carrier generation becomes significant.

Since dot location is not precisely controlled, it is important that channel surface potential in the active region be uniform. Otherwise the V_{th} shift from charge stored in dot will vary with dot location. Figure 9a) shows the surface potential of channel in the active region (dashed lines indicate edge of inversion. electrode) as a function of control gate bias where inversion electrode is kept constant at 1V. In this case interesting properties are seen in the subthreshold region. The length of the active region can be defined as where the reduction in surface potential from nc-Si dot shielding of 20mV will result in a potential minima for the entire device. In the case of constant inversion gate bias, the length of active region increases from 50nm to the length of trench width 200nm. Thus V_{th} shifts due to shielding from charge stored in dots further from the center of the trench would occur at higher gate bias. For subthreshold operations this would lead to unacceptable variations between devices. However, operation in this mode offers to be a new tool in studying single charged defect sites since location of defect can be distinguished. The source of the changing active area length is a short channel effect from nearby inversion electrodes which is readily eliminated by ramping control gate and inversion gate at same time. Figure 9b) shows a uniform potential within trench throughout subthreshold region of

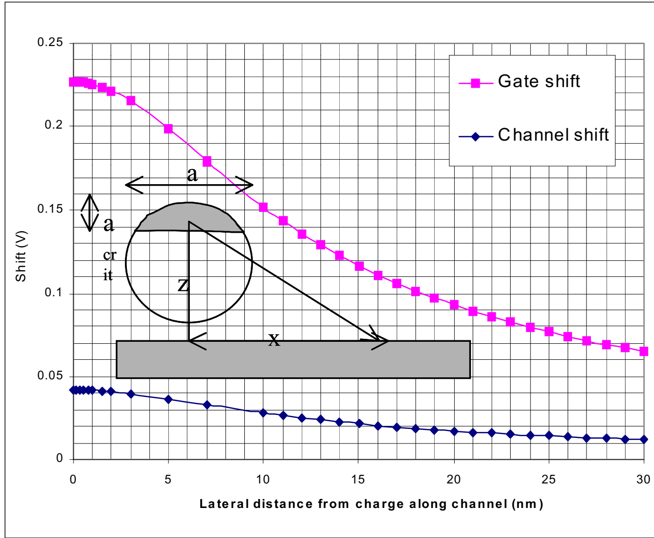


Figure 11. Calculated shift in surface potential and applied gate ptential due to single charge stored in nc-Si dot 10nm diamet as a function of lateral distance x along channel

gate bias. This allows for variation in dot location in different devices. Figure 10 shows the subthreshold swing and V_{th} as a function of trench width. With constant V_{ig}=0.5V, severe short channel effects are seen with decreased V_{th} and high subthreshold swing with narrow trench width. If inversion and control gate are ramped together then short channel effects are eliminated. Thus this device design can operate in two modes, the first with constant V_{ig} to study defect location and control I_{sat} and the second case with inversion and control gate ramped together for optimal device performance.

The V_{th} shift due to shielding is readily calculated from the surface integral of Coulomb's law (eqn. 2), where l is lateral distance on channel from charge, a is edge length of dot, ε permittivity of oxide.

$$\varphi = \int_{a/2}^{a/2}\int_{a/2}^{a/2} \frac{q/a^2}{4\pi\varepsilon_o\sqrt{(l+x)^2+y^2+z^2}}dxdy \qquad (2)$$

$$\frac{\hbar^2\pi^2 N_i^2}{2m^* a^2} = E_{Field}a_{crit} \qquad (3)$$

However it is necessary to account that charge will be located at the top (gate side) of dot. Simply equating quantum confinement energy with applied potential give location of charge (eqn 3) where a_{crit} is the confinement length, E_{field} is electric field from gate, m* effective mass of electron, N_i quantum level number. In this case charge is localized in top 2nm in subthreshold region.

Confining charge at the top of nc-Si is a strong benefit for retention time as the tunnel probability at 10nm is prohibitively small. During write erase charge will be located at the thin tunnel barrier allowing for both long retention time and short write/erase times. The vertical and lateral distance from charge in dot is used to calculate shielding. Expected shifts are from 70-120meV depending on dot location on channel. As shown in Figure 11.Variation in V_{th} shift is reduced with narrower channel.

III Conclusions

Work with nano-scale Si fabrication has shown several important features. Ballistic transport conductance oscillations shows that dimensional scale and defect level in this system is remarkably small. Using readily deposited nc-Si, clear Coulomb oscillations are observed as well as memory nodes. The use of a 2-gate structure allows the optimization of parameters for memory devices.

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