Nanofabrication of p-type GaAs by AFM-based surface oxidation process and its application to planar-type devices

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Abstract

An atomic force microscope (AFM) tip-induced direct nano-oxidation method was used to fabricate nanoscale p-GaAs oxide dots and wires. From the duty ratio dependence of aspect ratios of oxide dots, it was considered that optimization of an anodizing time per cycle of a pulsed voltage was necessary. The oxide could be etched by water. By adjusting both oxidation and etching process conditions, a groove with 40 nm width and 6 nm depth was successfully fabricated. From these results, it was clear that the aspect ratio of p-GaAs oxide could be improved using a pulsed voltage, and optimization of process conditions, particularly the frequency and duty ratio of a pulsed voltage, was necessary to obtain p-GaAs oxide with a high aspect ratio. Furthermore, this AFM oxidation technique was applied to the fabrication of planar-type p-GaAs (semiconductor)/oxidized p-GaAs(insulator) junction devices. The electrical properties of the device showed suppression of the current at around zero bias. The nonlinear current-voltage characteristics suggested that oxidized p-GaAs becomes an insulating barrier material for holes, and that the AFM oxidation technique is suitable for fabricating p-GaAs based planar-type devices.

1. Introduction

Scanning probe microscopes (SPMs), such as scanning tunneling microscopes (STMs) and atomic force microscopes (AFMs), are now routinely used as tools not only for observing surfaces but also fabricating nanoscale structures, by means of tip-induced oxidation of localized regions. The first report of tip-induced oxidation of silicon was a STM study by Dagata *et al.*[1)]. However, the AFM has become a more attractive method because it can be used to observe not only metals and semiconductors but also insulators, and it does not require a bias voltage for imaging. Recently, this AFM-based surface oxidation process has been intensively investigated for several kinds of semiconductors such as Si,[2-5)] GaAs[6-8)] and GaSb.[9,10)] Currently, this technology is attracting considerable attention as a new nanolithography method, which can be used for the fabrication of quantum-effect electronic devices.[8,10)]

In our previous study, we modified the shape of an AFM tip by using a scanning electron microscope (SEM)[11)] and fabricated p-GaAs and n-InGaP oxide wires,[12,13)] but their aspect ratios were less than 0.1. To adopt the oxide wires as integral parts of the device serving as effective tunnel barriers for carrier transport,[8)] further improvements of aspect ratios are needed.

In order to improve aspect ratios of the oxide, an AFM-based surface oxidation process, including voltage modulation,[3-5)] was employed for the surface modification of a p-GaAs substrate and a p-GaAs thin film layer

grown by metalorganic molecular beam epitaxy (MOMBE). This study was intended as a feasibility test for the fabrication of single hole transistors (SHTs) on semiconductor surfaces. Suitable materials for this application are heavily doped semiconductors, because their carrier concentrations are as high as in metals, and are free from the problem of surface depletion.[7)]

2. Experimental procedure

We fabricated heavily carbon-doped p-GaAs by MOMBE using a VG V-80H growth chamber. Trimethylgallium ($Ga(CH_3)_3$: TMG) and elemental As were used as a Ga and carbon source and an As_4 source, respectively. From our experiments, it was found that the hole concentration could be controlled by changing the growth temperature. At a growth temperature of about 390°C, we obtained p-GaAs with a hole concentration above $10^{21}cm^{-3}$ on a SI-GaAs substrate. Furthermore, the growth rate of the p-GaAs depended on the growth temperature, and increased from about 0.1 to 1.0μm/h with increasing growth temperature from 390 to 580°C. The details of the MOMBE growth of p-GaAs are described elsewhere.[7,14-16)]

A Zn-doped p-GaAs substrate with a hole concentration of $1.0\times10^{19}cm^{-3}$ and a carbon-doped p-GaAs thin film layer was locally oxidized in air at room temperature using a commercially available AFM unit. The tip of the AFM was Au-coated Si_3N_4 with a pyramidal shape with a base scale of 4μm. A pulse generator was used for the source of pulsed voltage, and a semiconductor parameter analyzer was also used for the source of constant voltage.

Anodization by the water on the sample surface can occur just below the AFM tip when a negative bias voltage is applied. By keeping a tip's position or scanning a tip, nanoscale oxide dots or wires were fabricated.

3. Results and discussion

Figure 1 depicts an AFM image of p-GaAs oxide dots fabricated by the AFM-based surface oxidation method using pulsed (V=±20 V, f=1 Hz, duty ratio=50%) or constant (V=20 V) voltage. The anodizing time is shown near each dot. An anodizing time means a sum of the time, when a negative voltage is applied to an AFM tip. This AFM image clearly shows that the aspect ratios of oxide dots are improved using pulsed voltages.

As shown above, the AFM oxide produced using pulsed voltage exhibits structural differences relative to the oxide fabricated using constant voltage, particularly oxides obtained using a pulsed voltage were thicker than those obtained using constant voltage. Similar results were reported by Perez-Murano *et al.*[4)] According to them, ac modulation neutralizes trapped charges at the Si/SiO_2 (SPM oxide) interface during the reset part of the cycle, so that the local field at the center of the growing feature remains intense. This process enables the growth of a thicker oxide.

The ratio between the time for anodizing and the time for neutralizing trapped charges should be optimized. The result of the optimization is shown in Figure 2, which shows the duty ratio dependence of aspect ratios of p-GaAs oxide dots. The applied bias voltage is ±10 V and the total anodizing time is 4 s. The definition of the duty ratio is as follows: if the negative bias voltage is applied for 0.1 ms per 1 ms cycle(f = 1000 Hz), the duty ratio of the pulse is 10%. Thus, a 100% duty ratio denotes the condition of the oxidation using constant voltage, which is indicated as ▲ in Fig. 2. It is clear from Fig. 2 that the optimized duty ratios are approximately 15%(f =

500Hz), 30%(f = 1000Hz) and 60%(f = 2000Hz). That is, 0.3 ms for oxidation time per cycle. Under such conditions, oxyanions react with GaAs effectively and produce an oxide dot with a higher aspect ratio.

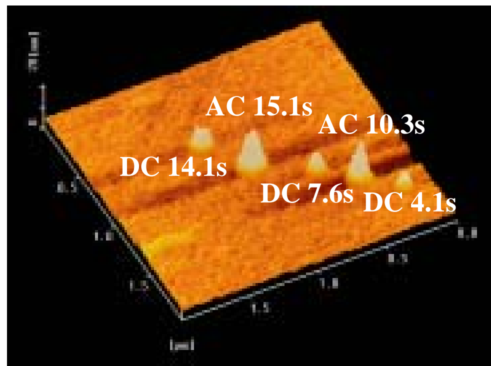

Fig. 1 AFM image of oxide dots fabricated using pulsed (V=±20V, f=1Hz, Duty ratio=50%) or constant (V=20V) voltage.

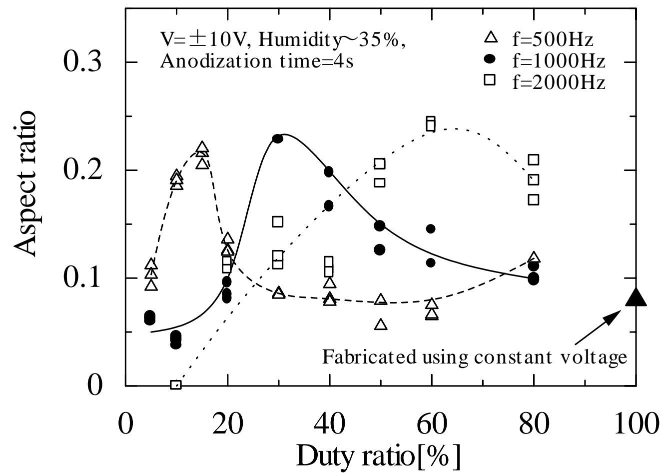

Fig. 2 Duty ratio dependence of aspect ratios of p-GaAs oxide dots fabricated using pulsed voltage.

Next, we used a pulsed voltage for the fabrication of oxide wires. This time the humidity around the AFM system was decreased to about 20% to reduce the width of oxide wires.[13)] After the fabrication, the p-GaAs sample was dipped in deionized water for 20 min in order to etch the oxide wires.[13)]

Figure 3 shows the scanning speed dependence of the aspect ratios of oxide wires and grooves fabricated using a pulsed (V=±8 V, f=1000 Hz, duty ratio=30%) voltage. From Fig. 3, it is clear that aspect ratios of oxide wires and grooves are improved by optimizing the scanning speed. As a result, we fabricated a p-GaAs groove with a 40 nm width and 6 nm depth at a scanning speed of 60 nm/s. Figure 4 shows the cross-sectional views of the wire (before etching) and the groove (after etching).

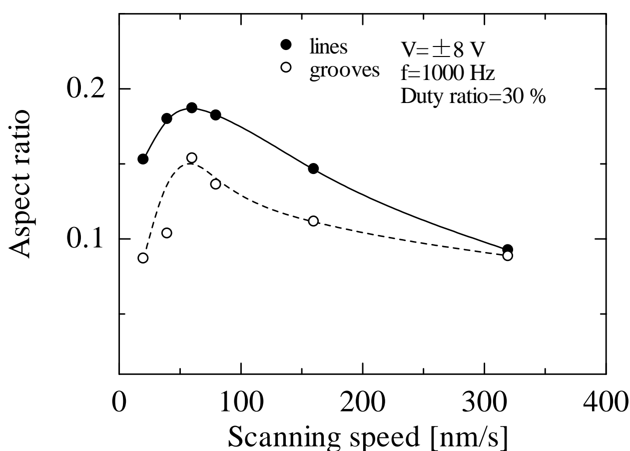

Fig. 3. Scanning speed dependence of aspect ratios of p-GaAs oxide wires and grooves fabricated using pulsed voltage.

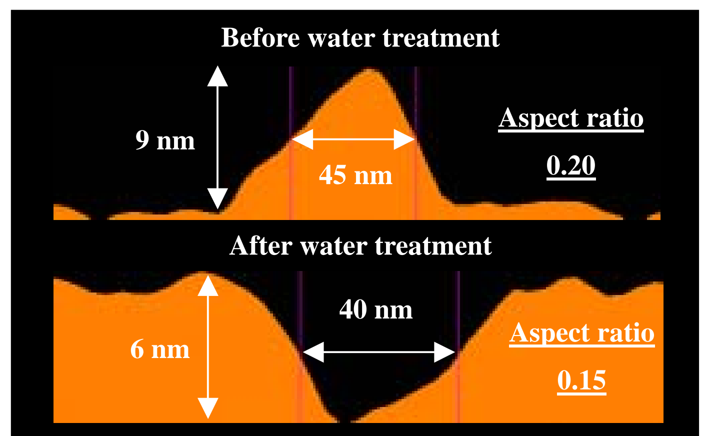

Fig.4 Cross-sectional views of a wire (before etching) and a groove (after etching) obtained using pulsed voltage.

This optimized scanning speed indicates the optimized anodizing time per definite oxide wire length. However, to understand the mechanism of the oxidation process during thp scanning, further experiments and theoretical analysis are needed.

This AFM oxidation technique was applied to the fabrication of planar-type p-GaAs (semiconductor)/oxidized p-GaAs (insulator) junction devices. A schematic view and an AFM image of the fabricated device are shown in Figure 5 and Figure 6, respectively. In this device, the white area shows the oxidized p-GaAs. At the center of the channel, there is an oxidized p-GaAs wire, which is formed using pulsed (V=±10 V, f=1000 Hz, duty ratio=30%) voltage and may act as a barrier insulator. The source and drain are placed in-plane and connected to the contact pads (Ag). The source-drain current-voltage characteristics of a device at room temperature without a barrier (indicated as "before") and with a barrier width of 40nm ("after") are shown in Figure 7. From this result, the current can be seen to be suppressed at around zero bias. These nonlinear current-voltage characteristics suggest that the oxidized p-GaAs formed by AFM oxidation acts as an insulating barrier material for holes, and that p-GaAs based planar-type semiconductor-insulator-semiconductor (SIS) devices can be obtained using the AFM oxidation technique.

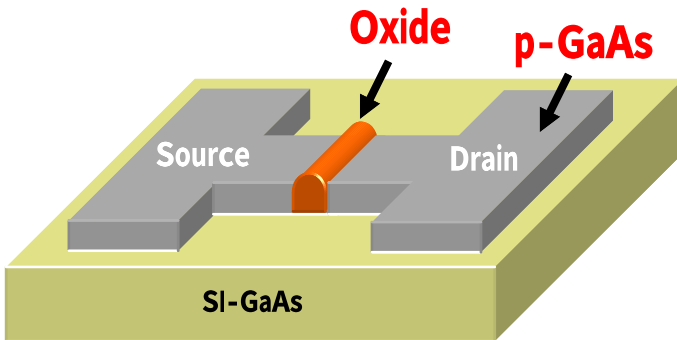

Fig. 5. Schematic view of a planar-type p-GaAs based SIS device.

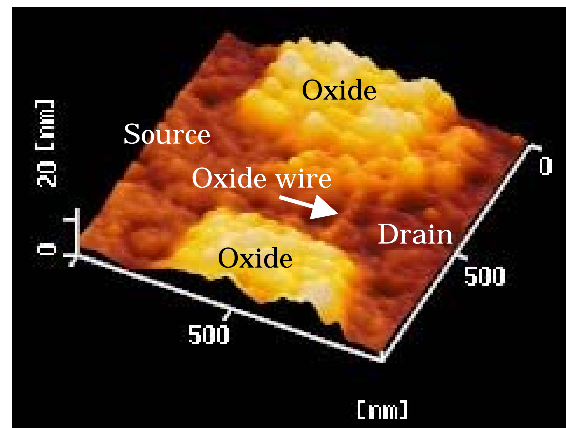

Fig.6 An AFM image of a planar-type p-GaAs based SIS device.

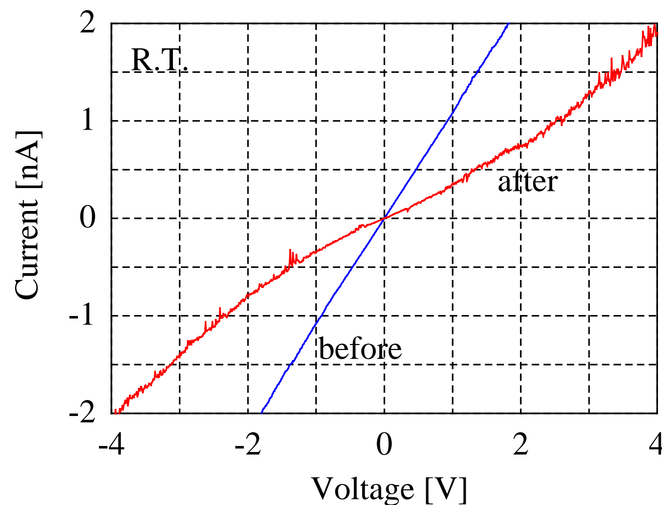

Fig.7 The source-drain current-voltage characteristics at room temperature. ("before" : before fabricating oxide; "after" : after fabricating oxide)

4. Conclusions

We have successfully fabricated nanoscale p-GaAs oxide dots and wires by an AFM-based surface oxidation process using pulsed voltage. From the duty ratio dependence of the aspect ratios of oxide dots, it was considered that optimization of an anodizing time per cycle of pulsed voltage was necessary. The order of the optimized time for negative part of a pulsed voltage is 0.3ms for GaAs oxidation. As a result, we fabricated a p-GaAs groove with a 40 nm width and 6 nm depth at a scanning speed of 60 nm/s. From these results, it is clear that a pulsed voltage can be employed for the fabrication of oxide dots and wires with a high aspect ratio. Furthermore, planar-type p-GaAs based SIS devices were fabricated using an AFM oxidation technique with voltage modulation. The electrical properties of the device showed suppression of the current at around zero bias. The nonlinear current-voltage characteristics suggest that oxidized p-GaAs becomes an insulating barrier material for holes, and that the AFM oxidation technique is suitable for fabricating p-GaAs based planar-type SIS devices.

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