IEICE TRANS. ELECTRON., VOL.E84–C, NO.10 OCTOBER 2001

PAPER *Joint Special Issue on Heterostructure Microelectronics with TWHM 2000*

InP DHBT with 0.5 μm Wide Emitter along $\langle 010 \rangle$ Direction toward BM-HBT with Narrow Emitter

Toshiki ARAI[†], **Shigeharu YAMAGAMI**[††], **Yoshifumi OKUDA**[††], **Yoshimichi HARADA**[††], ***Nonmembers***, **Yasuyuki MIYAMOTO**[†a)], ***and*** **Kazuhito FURUYA**[†], ***Regular Members***

SUMMARY Fabrication process for narrow emitter along $\langle 010 \rangle$ direction in heterojunction bipolar transistor fully drawn by electron beam lithography was studied. Emitter structure of a 100 nm width was formed by using epitaxial structure with 30-nm-thick InP layer of emitter. Transistor operation of devices with 0.5-μm-wide emitter was confirmed. This process can be applied to a buried metal heterojunction bipolar transistor (BM-HBT) with narrow emitter, resulting in high-speed operation of BM-HBT.

key words: *InP, HBT, narrow emitter*

1. Introduction

In heterojunction bipolar transistors (HBTs), reduction of total base-collector capacitance (C_{BCT}) is effective in the improvement of high-speed operation. To reduce C_{BCT} in HBTs, implanted base extrinsic regions [1], undercutting collector and subcollector layers [2], buried subcollector using selective growth [3] and a transferred-substrate process [4] have been previously demonstrated. We proposed buried metal heterojunction bipolar transistor (BM-HBT), in which tungsten stripe with a same width of emitter mesa is buried under a collector layer of non-doped InP and there is no conductive layer under the extrinsic base region [5]. BM-HBT with emitter width of 2 μm was fabricated and reduction of C_{BCT} was confirmed [6]. Maximum oscillation frequency (f_{MAX}) and current gain cutoff frequency (f_{T}) of BM-HBT were estimated [5]. Calculated dependence on emitter width shows that f_{MAX} increase monotonously and f_{T} keeps at constant value even when emitter width is reduced to 100 nm. Thus, fabrication process of fine emitter narrower than 1 μm width is essential for BM-HBT. To bury tungsten stripe by InP layer by using organmetallic vapor phase epitaxy (OMVPE), direction of the tungsten stripe must be along $\langle 010 \rangle$ direction [7]. So, emitter mesa for BM-HBT must be formed along $\langle 010 \rangle$ direction. The emitter mesa, which is formed along this direction, has a (001) plane and a (010) plane at mesa side. Undercut etching of InP layer with (001) and (010) plane is much faster than that with (011) or (01$\overline{1}$) plane, which are side plane of emitter mesa along $\langle 01\overline{1} \rangle$ or $\langle 011 \rangle$ direction [8]. This property has a difficulty in control of length of undercut etching, although it has a possibility to fabricate fine emitter. Another difficulty of fabrication process is an alignment between buried metal wire and emitter mesa. When size of each becomes finer, required process becomes difficult. As a result, fabrication process of narrow emitter along $\langle 010 \rangle$ direction and the process that enables to align the emitter mesa with the buried metal before-and-after the growth are required. To confirm the feasibility of first step, conventional HBT with narrow emitter must be fabricated.

In this report, fabrication process of narrow emitter along $\langle 010 \rangle$ direction is described. Thickness of an InP layer of emitter was reduced to 30 nm. By control of length of undercut etching, a 100-nm-wide emitter was fabricated when width of an emitter metal was 400 nm. By using these processes, conventional HBT with 500-nm-wide emitter along $\langle 010 \rangle$ direction was fabricated.

2. Fabrication Process for Narrow Emitter

For fabrication of emitter structure, there are dry etching and wet chemical etching as etching method. In case of dry etching, etching time, which controls etching depth, must be exactly decided because of low selectivity of material. In case of wet chemical etching, it has a good property in selectivity, but undercut etching of an InP layer do not stop when emitter finger orient along $\langle 010 \rangle$ direction. This property has a possibility to fabricate a fine emitter mesa narrower than emitter electrode, if the length of undercut etching is intentionally controlled. Thus, wet chemical etching was selected for fabrication of emitter structure.

To shorten the length of undercut etching, the InP layer must be thin because lateral undercut etching of InP layer is faster than vertical etching. Reduction of the emitter thickness has a possibility to decrease current gain. So, the current gain of HBTs with thinner InP layer was examined. Five HBTs structure with different thickness of InP layer were grown

Manuscript received November 3, 2000.
Manuscript revised May 30, 2001.

[†]The authors are with the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, 152-8552 Japan.
[††]The authors were with the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, 152-8552 Japan.
a) E-mail: miya@pe.titech.ac.jp

Table 1 Epitaxial layers of HBTs. Five different emitter structures were fabricated.

Layer	Material	Doping [cm^{-3}]	Thickness [nm]				
Contact	n-GaInAs	2×10^{19}	20				
Emitter	n-InP	2×10^{19}	5	5	5	5	70
	n-InP	5×10^{17}	15	25	45	100	100
Base	p-GaInAs	2×10^{19}	50				
Collector	i-GaInAs	—	60				
	n-InP	5×10^{17}	5				
	i-InP	—	200				
Subcollector	n-GaInAs	1×10^{19}	600				

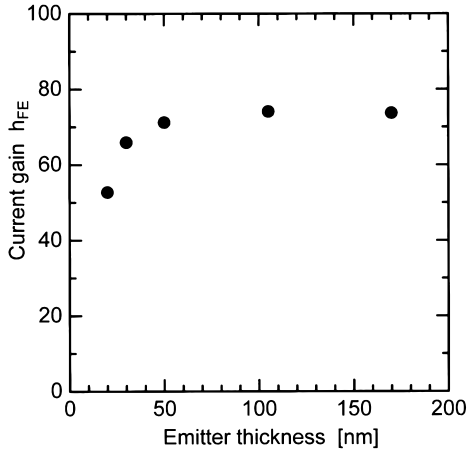


Fig. 1 Dependence of current gain on emitter thickness of InP layer. Emitter area was $50 \times 50\,\mu m^2$.

on (100) InP substrate by OMVPE, as shown in Table 1. Emitter layer consisted of a heavy-doped InP layer ($n = 2 \times 10^{19}\,cm^{-3}$) and a light-doped InP layer ($n = 5 \times 10^{17}\,cm^{-3}$). The thickness of the heavy-doped layer was 5 nm and that of the light-doped layer was changed from 15 nm to 100 nm. The epitaxial structure, which consisted of a 100-nm-thick heavy-doped layer and a 70-nm-thick light-doped layer, was also grown as a reference. Emitter mesa and base mesa were patterned by photolithography and formed by wet chemical etching. Photo-resist was used as a mask at etching. A solution of HCl:H_3PO_4=1:1 and a solution of a citric acid:H_2O_2=5:1 were used for the etching of InP layer and GaInAs layer, respectively. The area of emitter mesa was $50 \times 50\,\mu m^2$. After mesa formation, a 10-nm-thick Cr and 100-nm-thick Au were evaporated on the emitter mesa, the base mesa and the subcollector layer as electrodes. Common-emitter collector I-V characteristics of the fabricated devices were measured. Figure 1 shows the current gain of HBTs at collector voltage of 1.5 V as a function of thickness of the InP layer. Current gain was 74 when the InP layer was enough thick. When emitter thickness was less than 30 nm, current gain decreased. However, current gain of 53 could be obtained when total InP thickness was 20 nm.

Current gain was decreased with reduction of emitter thickness when the thickness was thinner than 30 nm. Current gain is decided by a product of emitter injection efficiency and base transport efficiency. Base transport efficiency was not dependent on emitter thickness. So, it was suggested that reduction of current gain was caused by reduction of emitter injection efficiency. The injection efficiency is reduced when p-n junction is not located on InP/GaInAs hetero-interface. By reduction of the thickness of the light-doped InP layer, heavy-doped InP layer was close to base layer. Thus, abnormal Zn diffusion into InP layer may be enhanced by reduction of emitter thickness [9], [10]. Measured turn-on voltage of common-emitter collector I-V characteristics, which indicate place of junction, was decreased with reduction of emitter thickness. This tendency can be explained by moving of the place of junction into base layer. Measured shift of turn-on voltage did not agree with the assumption of abnormal Zn diffusion. Another explanation for the measured dependence on emitter thickness is tunneling. InP layer of emitter works as a barrier for hole to tunnel from a base layer to an emitter contact layer. Tunneling probability is increased with reduction of emitter thickness, resulting in increase of base current. By reduction of InP layer thickness, tunneling probability of electrons from emitter layer to base layer is also enhanced, and turn-on voltage has possibility to decrease. To explain the cause of reduction of current gain, more precise calculation is essential with taking location of the junction and tunneling into account.

To control the length of undercut etching, it is preferable that etching rate is slow and etched plane has a flat surface. So, an acid solution for etching was kept at low temperature. Narrow emitter mesa was formed by using the epitaxial structure with emitter thickness of 30 nm. A emitter metal with 20-nm-thick Ti, 25-nm-thick Pt and 200-nm-thick Au was formed by liftoff technique using electron beam lithography (EBL). Poly-methyl-methacrylate (PMMA) was used as resist. A GaInAs layer and an InP layer were etched by solutions of a citric acid:H_2O_2=5:1 and HCl:CH_3COOH=1:4 which were cooled at a temperature of 3–5°C, respectively. The length of undercut etching for the GaInAs layer was 50 nm when etching time was 90 sec, and the length of undercut etching for the InP layer was 100 nm when etching time was 30 sec. Total length of undercut etching restrained was 150 nm. The emitter structure with 100-nm-wide mesa could be formed when width of the emitter metal was 400 nm, as shown in Fig. 2.

To connect the narrow emitter metal, contact window on an insulation layer must be narrower than emitter metal. It is preferable that thickness of insulation layer on the emitter metal is thin and surface of the insulation layer is flat. So, benzocyclobutene (BCB) was used as the insulation layer. BCB layer was formed by spin coating and thermal curing at 250°C under a

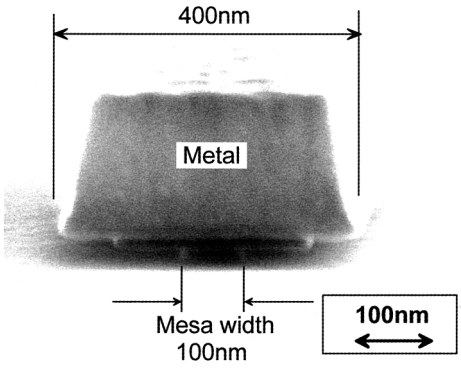


Fig. 2 SEM photography of the test structure of emitter. Mesa width was 100 nm. Mesa was oriented along ⟨010⟩ direction.

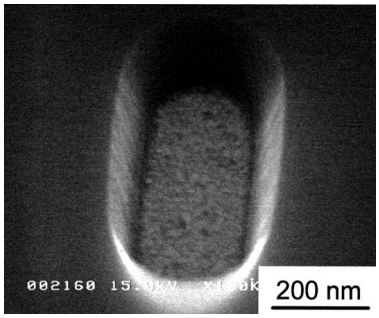


Fig. 3 SEM photography of the opened contact window on BCB layer. Width of the window was 200 nm.

N_2 atmosphere. The thickness of the BCB layer on emitter metal was 100 nm. ZEP520 has high resistivity for reactive ion etching (RIE), but ZEP520 layer cannot be formed on BCB layer directly because of its low adhesive property. PMMA can be spun on the BCB layer and ZEP520 layer can be formed on the PMMA layer. So, double-layer resist that consisted of a 60-nm-thick PMMA layer and a 400-nm-thick ZEP520 layer was formed [11]. Contact window was patterned by EBL. BCB was etched by RIE etching at 100 W and 5 Pa for 90 sec, in which mixed gas of CF_4:O_2=1:1 was used as etching gas. Contact window with a 200 nm width was formed, as shown in Fig. 3. Accuracy of alignment in EBL was less than 100 nm. A 200-nm-wide contact window can be aligned with 400-nm-wide emitter electrode, which can form 100-nm-wide emitter mesa.

3. Fabrication of Conventional HBT with Narrow Emitter

Five HBTs with different emitter widths were fabricated. Areas of emitter mesas were $0.1 \times 0.5\,\mu m^2$, $0.3 \times 1.5\,\mu m^2$, $0.5 \times 2.5\,\mu m^2$, $1.0 \times 5.0\,\mu m^2$ and $2.0 \times 10.0\,\mu m^2$. Areas of base mesas were $3.0 \times 4.4\,\mu m^2$, $3.2 \times 5.4\,\mu m^2$, $3.4 \times 6.4\,\mu m^2$, $3.9 \times 8.9\,\mu m^2$ and $4.9 \times 13.9\,\mu m^2$. EBL was used for patterning completely through the process. When base mesa was formed by wet chemical etching, base metal was used as a mask, and emitter mesa must be protected by resist. When device was isolated, emitter and base mesa must be protected, similarly. RD2000N was used for protection of the mesa structure as a negative type resist. Devices were buried in BCB layer for passivation and planarization.

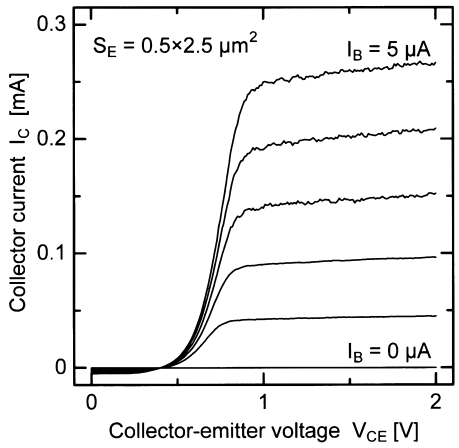


Fig. 4 Common-emitter collector I-V characteristics of fabricated HBT. Emitter mesa area was $0.5 \times 2.5\,\mu m^2$.

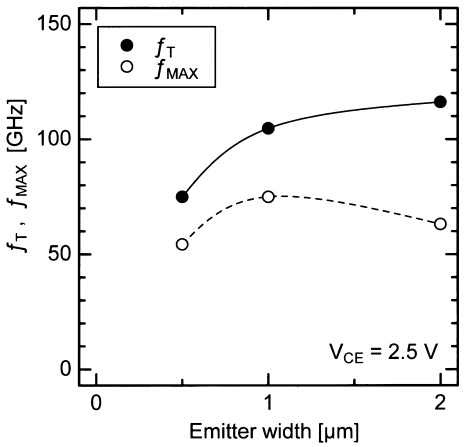


Fig. 5 Dependence of f_T and f_{MAX} on emitter width.

In the DC measurement, operation of transistor was confirmed with the emitter width of 500 nm, 1 μm and 2 μm. Figure 4 shows the common-emitter collector I-V characteristics of the device with 500-nm-wide emitter. Current gain of 50 was observed at collector voltage of 2 V and collector current of 0.25 mA. Microwave S-parameters were measured from 50 MHz to 30 GHz using an HP8722 network analyzer. f_T and f_{MAX} were extrapolated from current gain, $|h_{21}|$, and Mason's unilateral gain, U, respectively. f_T of 124 GHz was measured at the device with emitter width of 2 μm. f_{MAX} of 86 GHz was measured with emitter width of 1 μm. Figure 5 shows the measured dependence of f_T and f_{MAX} on emitter width. f_T was decreased with reduction of emitter size. f_{MAX} showed a peak point around the emitter width of 1 μm.

f_{T} and f_{MAX} can be estimated by following equations.

$$\frac{1}{2\pi f_{\mathrm{T}}} = \tau_{\mathrm{b}} + \tau_{\mathrm{c}} + \frac{nkT}{qI_{\mathrm{E}}}\left(C_{\mathrm{BE}} + C_{\mathrm{BCT}}\right) + \left(R_{\mathrm{EE}} + R_{\mathrm{CC}}\right) C_{\mathrm{BCT}} \quad (1)$$

$$f_{\mathrm{MAX}} = \sqrt{\frac{f_{\mathrm{T}}}{8\pi R_{\mathrm{B}} C_{\mathrm{BCin}}}} \quad (2)$$

By the change of the emitter size, the relation between three capacitances is changed. Emitter-base capacitance C_{BE} and total base-collector capacitance C_{BCT} are promotional to emitter mesa area and base mesa area, respectively. An area, which is proportional to intrinsic base-collector capacitance C_{BCin}, is defined by an area closed by transfer length (L_{T}) of base electrode including emitter mesa area [12]. The value of $C_{\mathrm{BCT}}/C_{\mathrm{BE}}$ is increased with reduction of emitter size, because the ratio of area of base mesa to emitter mesa is not constant with reduction of emitter size. Hence, the emitter charging time become long. Collector charging time is also become long because of increase of the value of $C_{\mathrm{BCT}}/C_{\mathrm{BE}}$. Intrinsic transit time is not dependent on emitter size. So, f_{T} is reduced by reduction of emitter size. This explanation shows a good agreement with measured emitter width dependence of f_{T}. The value of C_{BCin} is reduced with reduction of emitter size and a product of base resistance R_{B} and C_{BCin} is also reduced. When the length of emitter width is close to the sum of L_{T} and separation between emitter mesa and base electrode (L_{g}), the $R_{\mathrm{B}}C_{\mathrm{BCin}}$ is saturated because $L_{\mathrm{T}}+L_{\mathrm{g}}$ is not dependent on emitter size. Thus, f_{MAX} is increased with reduction of emitter size by reduction of the $R_{\mathrm{B}}C_{\mathrm{BCin}}$ when emitter size is larger than $L_{\mathrm{T}} + L_{\mathrm{g}}$. f_{MAX} is reduced with reduction of emitter size due to reduction of f_{T} when emitter width is close to $L_{\mathrm{T}} + L_{\mathrm{g}}$. To estimate f_{MAX}, R_{B} is assumed which is inversely proportional to emitter length, and C_{BCin} is calculated using L_{T} of 0.59 μm and L_{g} of 0.45 μm. Using R_{B}, C_{BCin} and measured f_{T}, estimated f_{MAX} shows a good agreement with the measured dependence on emitter width.

We could not observe the operation of the devices with 100-nm and 300-nm-wide emitter, because a thickness of BCB around the devices has a slight dependence on mesa size, and the thickness of small area devices became too thin. Thus, opening of contact window adjusted for the narrow emitter will provide the operation.

4. Conclusion

Fabrication process of narrow emitter that oriented along ⟨010⟩ direction was studied. Emitter width of 100 nm was fabricated by using the HBT layer structure with emitter thickness of 30 nm. Using this process, conventional HBT with emitter width of 500 nm was fabricated and transistor operation was confirmed. By application of this process to fabricate BM-HBT with narrow emitter, high-speed operation of BM-HBT will be expected.

Acknowledgement

The authors would like to thank Profs. S. Arai, M. Asada and M. Watanabe of Tokyo Institute of Technology for useful discussion and encouragement. This work was supported by the Ministry of Education, Science, Culture and Sports through a Scientific Grant-In-Aid and the Research Center for Ultra-High-Speed Electronics and by the "Research for the Future" Program #JSPS-RFTF96P00101 of the Japan Society for the Promotion of Science (JSPS).

References

[1] P.M. Asbeck, D.L. Miller, R.J. Anderson, and F.H. Eison, "GaAs/(Ga, Al)As heterojunction bipolar transistors with buried oxygen-implanted isolation layers," IEEE Electron Device Lett., vol.EDL-5, no.8, pp.310–312, 1984.

[2] Y. Miyamoto, J.M.M. Rios, A.G. Dentai, and S. Chandrasekhar, "Reduction of base-collector capacitance by undercutting the collector and subcollector in GaInAs/InP DHBT's," IEEE Electron Device Lett., vol.17, no.3, pp.97–99, 1996.

[3] M.R. Frei, J.R. Hayes, J.-I. Song, H.M. Cox, and C. Caneau, "Selective growth of InGaAs/InP heterojunction bipolar transistors with a buried subcollector," Appl. Phys. Lett., vol.61, issue.10, pp.1193–1195, 1992.

[4] U. Bhattacharya, M.J. Mondry, G. Hurtz, I.-H. Tan, R. Pullela, M. Reddy, J. Guthrie, M.J.W. Rodwell, and J.E. Bowers, "Transferred substrate Schottky-collector heterojunction bipolar transistors: First results and scaling laws for high f_{max}," IEEE Electron Device Lett., vol.16, no.8, pp.357–359, 1995.

[5] T. Arai, H. Tobita, Y. Harada, M. Suhara, Y. Miyamoto, and K. Furuya, "Proposal of buried metal heterojunction bipolar transistor and fabrication of HBT with buried tungsten," Proc. 11st International Conference on Indium Phosphide and Related Materials, pp.183–186, May 1999.

[6] T. Arai, Y. Harada, S. Yamagami, Y. Miyamoto, and K. Furuya, "Frist fabriation of GaInAs/InP buried metal heterojunction bipolar transistor and reduction of base-collector capacitance," Jpn. J. Appl. Phys., vol.39, pt.2, no.6A, pp.L503–L505, 2000.

[7] T. Arai, H. Tobita, Y. Harada, M. Suhara, Y. Miyamoto, and K. Furuya, "Toward nano-metal buried structure in InP—20 nm wire and InP buried growth of tungsten," Physica E, vol.7, pp.896–901, 2000.

[8] Y. Matsuoka, S. Yamahata, K. Kurishima, and H. Ito, "Ultrahigh-speed InP/InGaAs double-heterojunction bipolar transistors and analyses of their operation," Jpn. J. Appl. Phys., vol.35, pt.1, no.11, pp.5646–5654, 1996.

[9] K. Kurishima, H. Nakajima, S. Yamahata, T. Kobayashi, and Y. Matsuoka, "High-performance Zn-doped-base InP/InGaAs double-heterojunction bipolar transistors by metalorganic vapor phase epitaxy," Appl. Phys. Lett., vol.64, no.9, pp.1111–1113, 1994.

[10] W.S. Hobson, S.J. Pearton, and A.S. Jordan, "Redistribution of Zn in GaAs-AlGaAs heterojunction bipolar transistor structure," Appl. Phys. Lett., vol.56, no.12, pp.1251–1253, 1990.

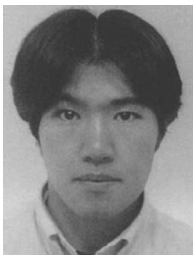
[11] Y. Miyamoto, A. Kokubo, H. Oguchi, M. Kurahashi, and K. Furuya, "Fabrication and transport properties of 50-nm-wide Au/Cr/GaInAs electrode for electron wave interference device," Applied Surface Science, vol.159–160, pp.179–185, 2000.
[12] K. Kurishima, "An analytic expression of f_{max} for HBT's," IEEE Trans. Electron Device, vol.43, no.12, pp.2074–2079, 1996.



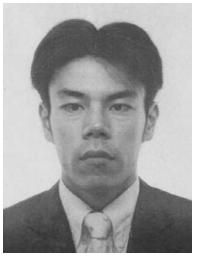
Toshiki Arai was born in Nagano, Japan, on November 13, 1973. He received the B.S. and M.S. degrees in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1997 and 1999, respectively. He is now working toward Ph.D. degree at the Tokyo Institute of Technology, with research focused on InP based HBT with buried tungsten wires by organometallic vapor phase epitaxy. Mr. Arai is a member of the Japan Society of Applied Physics. He received a Young Scientist Award for the Presentation of an Excellent Paper, in the 47th Spring Meeting of the Japan Society Applied Physics, in March 2000.



Shigeharu Yamagami was born in Osaka, Japan, on April 4, 1975. He received the B.S. and M.S. degrees in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1999 and 2001, respectively. During the master course, he studied fabrication process of HBT by electron-beam lithography. He joined NEC corp. in April 2001. Mr. Yamagami is a member of the Japan Society of Applied Physics.



Yoshifumi Okuda was born in Tochigi, Japan, on October 30, 1976. He received the B.S. degrees in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2000. He is now working toward M.S. degree at the Department of Information Processing, Tokyo Institute of Technology, with research focused on ultra-short-channel SOI MOSFET's.



Yoshimichi Harada was born in Tokyo, Japan, on January 9, 1975. He received the B.S. degree in electrical and electronic engineering and M.S. degree in physical electronics engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1998 and 2000, respectively. During the master course, he studied fabrication of HBT with buried tungsten wires. He joined NEC corp. in April 2000. Mr. Harada is a member of the Japan Society of Applied Physics.



Yasuyuki Miyamoto was born in Tokyo, Japan, on February 12, 1961. He received the B.S., M.S. and Ph.D. degrees in Physical Electronics from Tokyo Institute of Technology, Tokyo, Japan, in 1983, 1985 and 1988, respectively. In 1988, he joined the department of Physical Electronics, Tokyo Institute of Technology, as a Research Associate. In 1992, he became an Associate Professor with the Department of Electrical and Electronics Engineering. From 1994 to 1995, he was with AT&T Bell laboratories, Holmdel, NJ, U.S.A. as the visiting researcher. He is presently engaged in research on III-V semiconductor electronic devices and nanometer fabrication technology. Dr. Miyamoto is a member of the Japan Society of Applied Physics and the IEEE.



Kazuhito Furuya was born in Japan in 1948. He received the B.S., M.S. and Ph.D. degrees all from Tokyo Institute of Technology, Tokyo, Japan, in 1970, 1972 and 1975, respectively. He worked in Tokyo Institute of Technology on optical fibers, semiconductor lasers in the optical communication area. From 1980 to 1982, he was a consultant at Bell Laboratories, Holmdel, NJ, where he worked on semiconductor integrated optics. He is currently a professor in the Department of Electrical and Electronics Engineering, Tokyo Institute of Technology, working on the hot electron transport, electron-wave phenomena, and nanometer physics and fabrication for quantum effect devices.